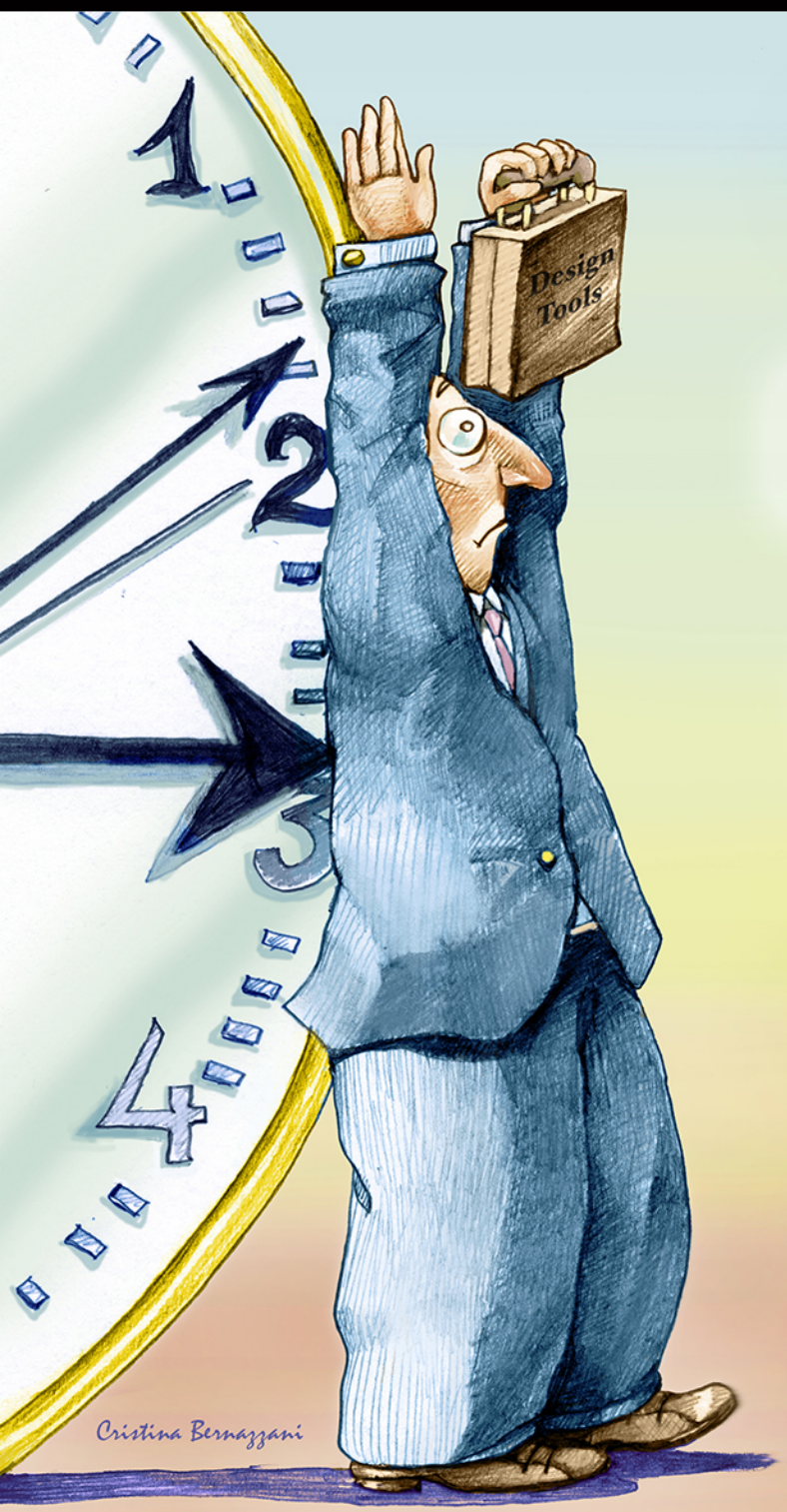
THE pcb design MAGAZINE

October 2015

an I·Connect007 publication



Don't Be Held Hostage by Design Cycle Time

by Scott Miller, page 12

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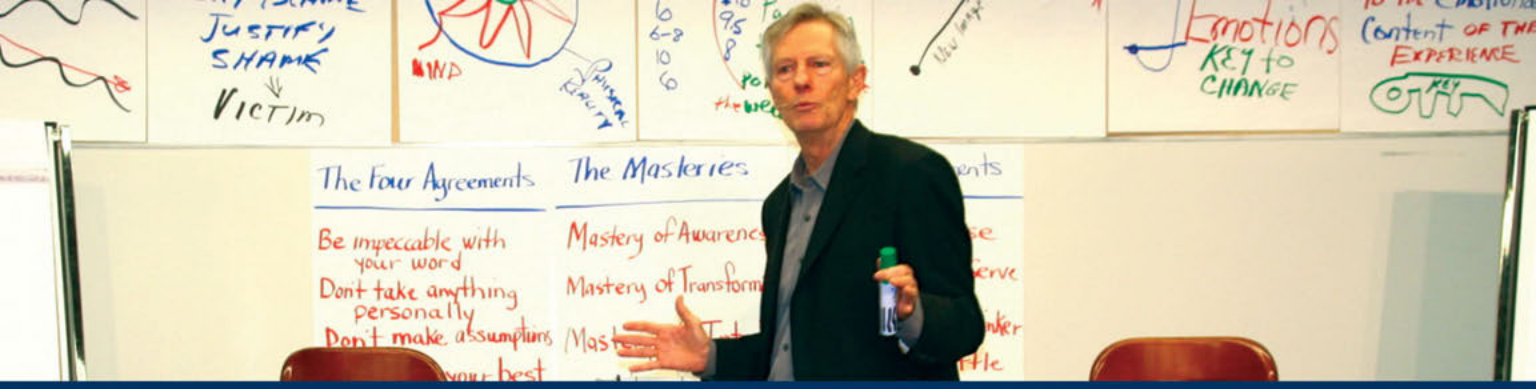

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October 2015

THIS MONTH'S FEATURE ARTICLES

Accelerating the PCB Design Cycle

As board speeds and densities continue to increase, it's becoming more difficult for PCB designers to shorten their design cycles and meet time-to-market demands. This month, we're featuring articles by Scott Miller of Freedom CAD Services, Bob Potock of Zuken, and Mark Thompson of Prototron Circuits, as well as tips from our subscribers on accelerating the PCB design cycle.

FEATURE COLUMN

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DK @ 10 GHz	3.45	3.00	3.45	2.80 - 3.45
Df @ 10 GHz	0.0030	0.0017	0.0031	0.0028 - 0.0036
CTE Z-axis (50 to 260°C)	2.90%	2.90%	2.80%	2.90%
T-260 & T-288	>60	>60	>60	>60
Halogen free	Yes	No	No	No
VLP-2 (2 micron Rz copper)	Standard	Standard	Available	Available
Stable Dk and Df over the temperature range	-55°C to +125°C	-40°C to +140°C	-55°C to +125°C	-55°C to +125°C
Optimized Global constructions for Pb-Free Assembly	Yes	Yes	Yes	Yes
Compatible with other Isola products for hybrid designs	Yes	Yes	Yes	For use in double-sided applications
Low PIM < -155 dBc	Yes	Yes	Yes	Yes

NOTE: Dk Df is at one resin %. The data, while believed to be accurate and based on analytical methods considered to be reliable, is for information purposes only. Any sales of these products will be governed by the terms and conditions of the agreement under which they are sold.

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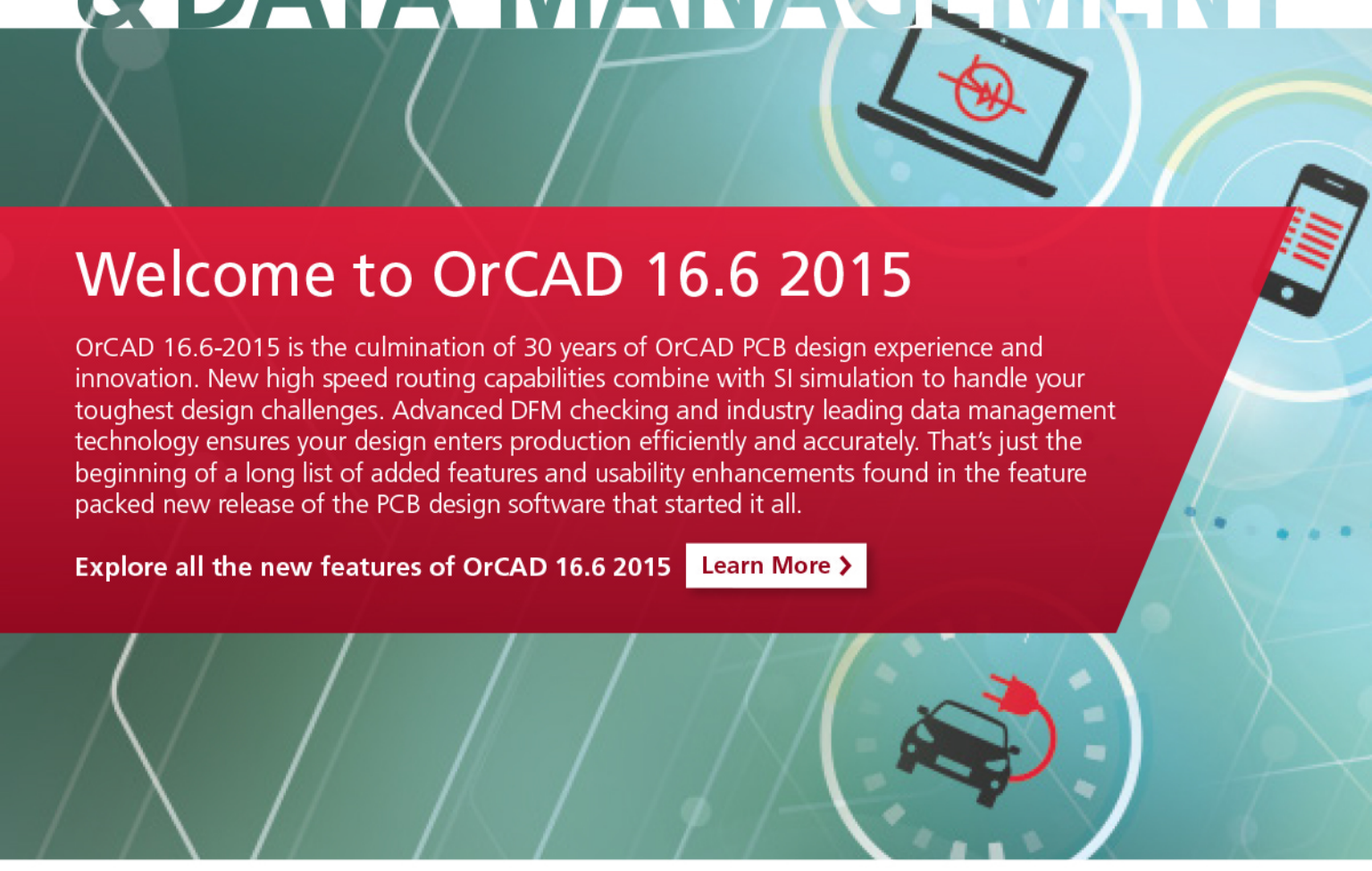
THE NEXT BIG THING IN PCB DESIGN INCLUDES SI SIMULATION HIGH SPEED ROUTING ADVANCED DFM CHECKING & DATA MANAGEMENT



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Squeezing Seconds Out of the Design Cycle

by Andy Shaughnessy
I-CONNECT007

It's almost that bad, isn't it?

When you're designing a board, time is always your enemy. Your deadline is around the corner, and you can't be late. (You're going to catch the blame anyway, even if it's not your fault.) So you constantly look for ways to shorten your design cycle, even if it means squeezing out a few seconds here and there.

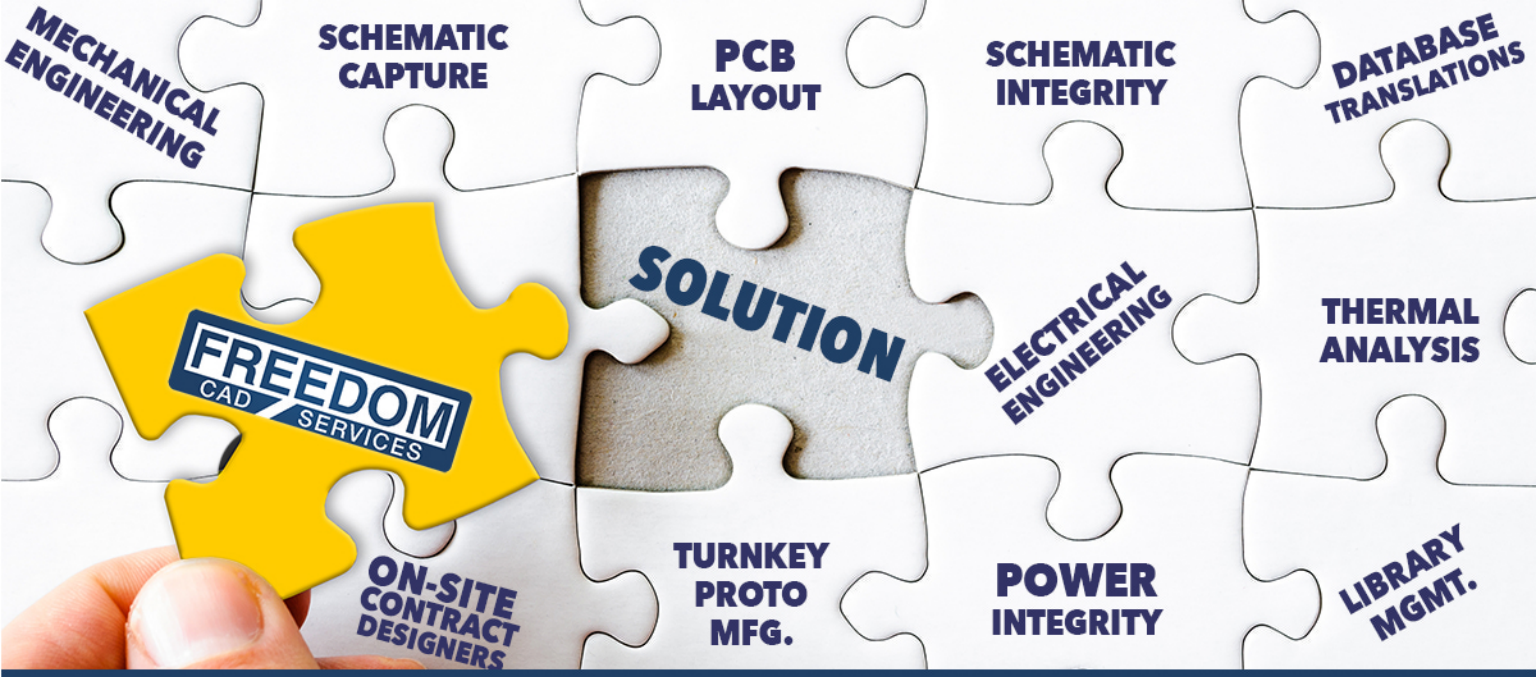
That's what we learned when we surveyed our readers recently. PCB designers said that time pressure was one of their least favorite parts of the job, and in some cases, they were ready to retire just to avoid design cycle challenges. I imagine that many of you near retirement, and that's quite a few of you, feel the same way.

In the survey, we started by asking readers to rank the importance of reducing their companies' PCB design cycles. A total of 88% ranked reducing the design cycle at least a 7 on a scale of 1–10.

We decided to cut to the chase. We asked, "What are the biggest bottlenecks in your PCB design cycle?" The answers were illuminating:

- The design is not ready for layout when we get it
- Schematic finalizations
- Customer unknowns
- Engineering changes
- Library updates
- Procurement of samples (a slow purchasing department)
- Footprint validation
- The PCB designer

Then we asked, "What tools or methods do you use to accelerate your design cycle?" I



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SQUEEZING SECONDS OUT OF THE DESIGN CYCLE

expected to hear about lines of spreadsheets or proprietary processes, but check out these replies:

- Do it right the first time
- Reuse of designs
- Mentor Xpedition
- Cadence Allegro
- PADS
- HyperLynx
- Use our normal app but try to stay on top of app improvements
- Inside tools
- Third-party software enhancements to CAD tools
- No unnecessary meetings— most are a waste of time
- CAD DRC rules
- CircuitSpace, script automation (dalTools), wearing multiple shirts, overtime
- 3D printers

After hearing many of you complain about your EDA tools for years, I was surprised to hear that some designers think their particular EDA software offers the best way to accelerate their design cycle.

(How are EDA tools like members of Congress? Many designers hate their EDA tools, but they like their particular tool, the same way Americans re-elect their Congressmen almost every election cycle despite claiming to despise Congressmen in general. The same attitude applies: "Well, mine is one of the good ones.")

We also asked, "How do you estimate design cycle time?" Here's how it broke down:

- 44.44% checked "Gut instinct based on experience"
- 27.78% checked "Spreadsheet"
- 5.56% checked "Estimator program"
- 22.22% checked "Other," with comments such as "programs and last project's history" and "estimate from two different designers and current workload"

Yes, almost half of respondents said they used, "Gut instinct based on experience."

How do you estimate your design cycle time?

So this month we have a variety of articles on accelerating the PCB design cycle. Scott Miller of Freedom CAD Services discusses how to use everything from keyboard shortcuts to third-party tools to squeeze time out of the design cycle. Bob Potock of Zuken explains how moving from discipline-centric to product-centric design techniques can speed up your process. Mark Thompson of Prototron Circuits offers his top 10 ways to accelerate the design cycle.

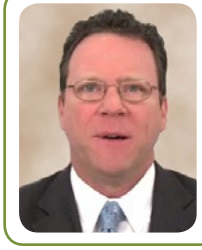
And I've written a short piece that features 10 tips, tricks and techniques sent in by subscribers from around the world. These tips should be extremely useful to PCB designers, and right away.

Invasion of the Drones

Yes, I-Connect007 has a new drone. And not just any drone: This one is equipped with a snazzy video camera. I want my own drone now.

We've already used the drone to shoot a flyby video of the equipment at Whelan Engineering for a feature article in the October 2015 issue of our sister magazine *The PCB Magazine*. To check out the video, click here.

See you next month! **PCBDESIGN**



Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 16 years. He can be reached by clicking here.

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Don't Be Held Hostage by Design Cycle Time

by Scott Miller
FREEDOM CAD SERVICES INC.

Mylar. Black tape. X-acto knives. Drafting tables. Ring lights.

These were the tools of the trade for the pioneers of printed circuit board design. Manually creating the large artwork that would then be photo-reduced to make the filmwork to image double-sided boards was truly an art form. The best designers were both neat and efficient. Somehow they avoided going home at night with their shirts or skirts covered with bits of tape stuck to them.

For those of you experienced designers, it's incredible to see how far the art of PCB design has come over these 40+ years of evolution. CAD software has replaced Mylar, and computer screens have replaced lighted drafting tables. And now, it's more science than art. PCB design now requires puzzle-solving skills on many levels to handle ever-increasing density and speed challenges.

The Need for Speed

By the mid-'90s, technologists were predicting that the use of conductive copper interconnections would need to be replaced with optics in order to address the increasing signal speeds. Year after year, the industry has found ways to increase the capabilities of copper interconnect to meet the escalating challenges. Some of these solutions were materials' improvements such as high-speed laminates, smooth copper foil, and high-speed connectors. But many were based on PCB design strategies, including the use of back-drilling, reference planes, differential pairs, length matching, hole, pad and anti-pad shapes and sizes. Engineers and designers use many other strategies to maximize performance while minimizing cost.

One thing is clear: Designing printed circuit boards today is much more complicated and challenging than ever. Designing today's leading-edge circuit boards requires that the designer:

- Has a strong knowledge of the capabilities of the CAD software.
- Understands PCB fabrication processes.
- Has a general knowledge of electronics and component functionality.
- Has a general knowledge of signal and power integrity.
- Understands PCB assembly processes.
- Understands industry specs.

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In addition to all of these challenges, designers have to be efficient three-dimensional puzzles solvers because time-to-market is still a vitally important objective. After all, time is money.

So how do today's designers balance the technical and timing demands? There isn't one answer. It requires efficient use of the CAD tools, floor planning and effective communication with all parties involved.

Fortunately, Cadence Design Systems, Mentor Graphics, Altium and other PCB CAD software developers continue to make great strides at improving the capabilities of PCB layout tools. This has made it much faster to route differential pairs, create shapes or replicate circuits. And while they strive to make user interfaces logical and easy to use, many capabilities aren't as obvious.

Today's designers must continue to study CAD tools to leverage these improvements. We request that our 30+ designers share time-saving or technique improvements that they discover with fellow designers to help drive efficiency within our service bureau.

"Beyond optimizing CAD tools, some third-party tools can be very helpful for driving efficiency by providing additional automation."

In addition to the inherent CAD tool capabilities, time saving features such as "alias" and "function" keys can be set up to save strokes and mouse travel time. With Cadence Allegro, you can use the CTRL _key within the command to capture additional functionality or right-click the mouse for additional functionality to expand/contract shapes, modify padstacks, place, replicate, alternate symbol, refresh symbol instances or create groups [1].

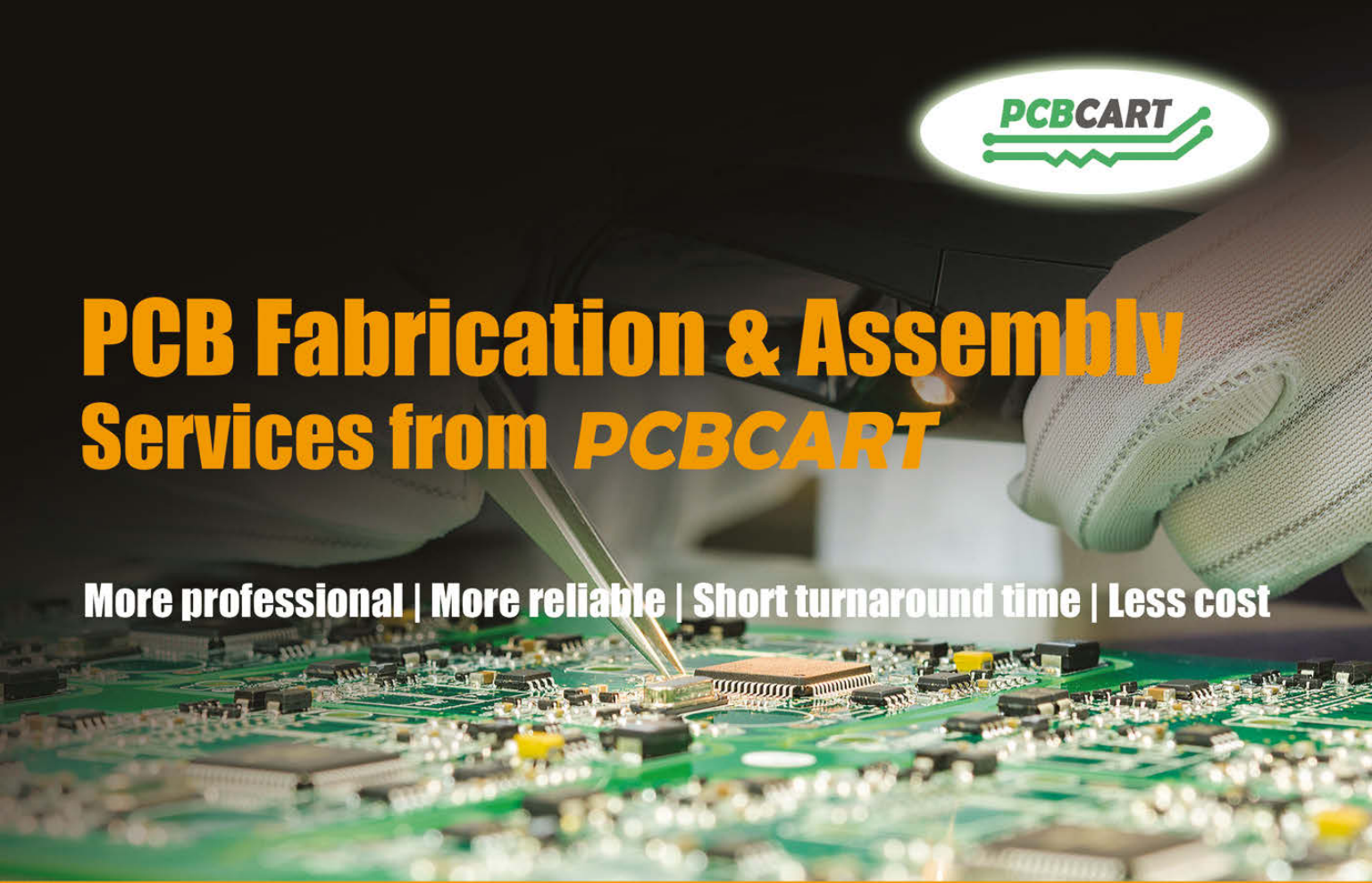
Beyond optimizing CAD tools, some third-party tools can be very helpful for driving efficiency by providing additional automation. One that we have found to be effective is dalTools, which works within Allegro to provide a variety of time-saving macro functions during the layout process. More than 80 commands are available in this tool, but some of the most frequently used are:

- Cut/Stretch
- Copy/Change
- Shapes (multiple features)
- Dangling Lines
- Place/Highlight (by schematic page)
- Compare
- Mirror
- GND ring/coax
- Silkscreen (checks)
- GND Fence
- Text
- Diff pair highlight
- Backdrill

Communication is a critical component of design efficiency, including how clearly defined the design requirements are, both mechanical and electrical. Poorly documented requirements can result in missed expectations and rework that can add time to the design effort. We are finding that more and more layout designers are working remotely from their engineer. Freedom CAD actually performs 99% of our layout support remotely from our customers' engineers. We, like many organizations, utilize Web conferencing tools such as WebEx, GoToMeeting and Google Hangout, to name a few. These tools enable screen-sharing and drawing, which greatly reduces the obstacles of working remotely. Web conferences can be set up in seconds by either party and enable real-time collaboration to view and talk through issues without resorting to lengthy e-mails, which can cause delays.

Kick-Off Time

When we are not local to the engineer, we use Web conferences to hold a kick-off meeting between the layout engineer and the electrical engineer and others related to the design, to walk through it. This provides the opportunity



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to visually share information and ask questions to learn what's critical and what's not from the customer, and to facilitate a smooth launch of the design process.

We like to request mechanical data from the customer in the form of EMN or 1:1 DXF files that can be imported into the CAD tool. This is more efficient and less prone to error. To assure that electrical rules are followed, we like to get the rules (match groups, max length, spacing for noisy signals, etc.) in a doc file or a spreadsheet so we can enter them into the constraint manager.

We also determine if previous designs or sections of the design can be reused. Reuse of a previous board outline, existing stack-up, and PCB fab and assembly drawings notes is a simple way to save time. Reusing prior circuit designs, such as power supplies or DDR routing, can save a significant amount of time. Again, third-party tools such as dalTools and EMA Design Automation's CircuitSpace make reuse in Allegro even more efficient. CircuitSpace can also be used to reduce placement time by AutoClustering functional groups of components.

> "We have found that component area placement and route studies can be very helpful to identify solutions in problem areas prior to tackling the complete board design."

We have found that component area placement and route studies can be very helpful to identify solutions in problem areas prior to tackling the complete board design. These efforts will enable the engineer and designer to work through the tradeoffs that are often required to resolve issues without the distractions of the peripheral items associated with the complete board design. When completed, the results of the placement or route studies can be used in the actual design and provide a faster and more predictable design cycle time to complete the board.

An area of communications that is often underappreciated, but has become vitally important to design efficiency, is the dialogue with the PCB fabricator. It's critical to engage the fabricator very early in the design process to nail down the proper materials and stack-up. With so many options for via structures, it is critical to select the most appropriate structure for the design. Adding blind and/or buried vias as an afterthought can limit their utilization and drive up the printed circuit board cost. The designers need to know if back drilling is a requirement in order to plan their routing strategies. We have seen many project timelines impacted by eleventh-hour negotiations between the engineer and fabricator for stack-ups and line width and spacing approvals. In addition, we highly recommend that the printed circuit board assembler be involved early in the process to review the placement file for DFM approval. It's much more efficient to make any component adjustments before the routing and delay tuning is implemented.

Flow planning is another area that can save time. We use Cadence's flow planner to help plan the routing on the various layers. It allows us to grab a "bundle" of traces and plan their track layer by layer, while taking into account how much room they will require based on their constraints. This provides a couple of efficiency benefits. One, it identifies bottlenecks in the planning stages, and two, the flow plan can be used to provide guidance to the designers who are doing the routing to support the lead designer.

Signal and power integrity analysis are key methods for assuring that the board design will meet the performance requirements on the first pass. By using software to simulate the effects on signal and power integrity, our customers spend less time in the lab trying to find out why their design isn't performing as expected. Performing in-process simulations enable problems to be identified and corrections to be made earlier in the design process, minimizing the collateral

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damage. The more items you have to move to address a problem, the more time this takes.

Pitching in to Save Time

This brings us to another methodology we use for accelerating the design cycle times. Our company is staffed with support designers on the first and second shift. These designers are trained to follow the same methodologies for pin escaping and routing. They work hand in hand and under the guidance of the lead designer to help reduce the design cycle time. Both Mentor and Cadence have developed partitioning tools to help manage this, but they are not required to successfully leverage multiple designers concurrently. What is required is crisp communications to manage the effort. Think of the lead designer as the conductor of an orchestra. Without his direction, the execution is not likely to meet the audience expectations.

Finally, generating a "clean" database to the PCB fabricator is critical to achieving the ultimate goal of the design process: getting boards in hand to debug. If there are DFM issues in the database, the fabricator will typically stop their process until the issues identified are addressed (fixed or waived). To optimize each customer's success when seamlessly releasing design databases to fabrication, we perform an independent QA and Valor analysis to validate every design. This extra step helps to assure that our customer's "release to fab" dates are not compromised with delays due to the fabricator addressing DFM issues.

On the horizon, the future is exciting for the layout designer. Mentor and Cadence are both developing their interactive autorouting capabilities. These features work with the designer's guidance to selectively autoroute and tune the signals. Both companies can provide examples of design cycle times that have been reduced by 20-40%.

Designers who have been in this industry since its earliest days have seen a lot of changes since the days of Mylar and tape. One thing is for sure: The dynamic developments in electronic packaging will continue to drive the development of new features in CAD tools to help minimize the design time.

One thing hasn't changed over the years: Time is still money. **PCBDESIGN**

References

1. More information about these features can be found in the presentation Designing More Efficiently.

Scott Miller is chief operating officer for Freedom CAD Services, responsible for the company's operations, sales and marketing. He has more than 37 years of experience in the electronics industry and has been with Freedom CAD since 2004. He can be reached by clicking here.

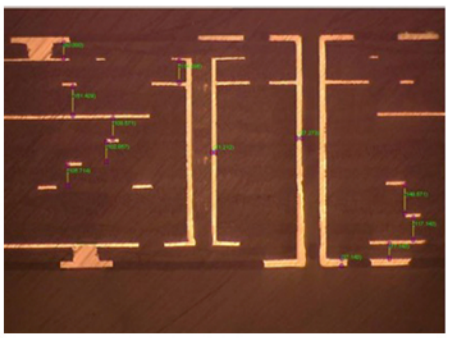
Whelen Engineering: The First New Captive in Decades?

The future of American manufacturing might be found in the small community of Charlestown, New Hampshire, at Whelen Engineering. Founded and headquartered in Connecticut in the 1950s, Whelen manufactures all things related to emergency lights and sirens for the automobile and aviation industries.

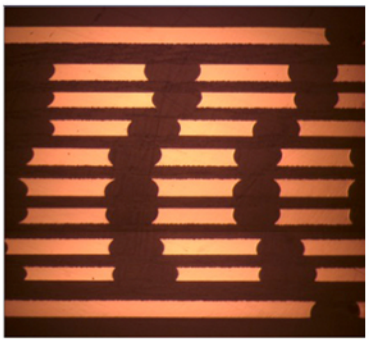
For years, Whelen had been spending about $7 million annually on PCBs from China, but being a strong advocate for bringing jobs and dollars back to the U.S., two years ago the firm decided to purchase its PCBs in America. Who did they choose as their new supplier? Well, that's where it gets interesting. Whelen chose to be its own PCB supplier. Click here to read the article in *The PCB Magazine.*

EXTRAORDINARY

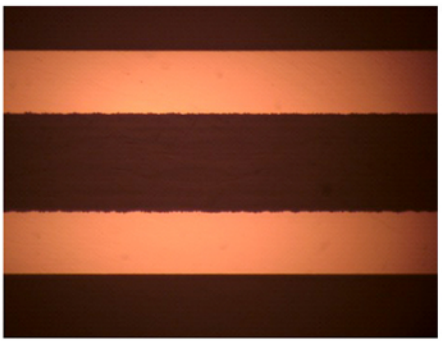
Heavy copper PCB – Microsection



Via in Pad Technology (Micro-via)



10 Layers: 140µm copper finished in each layer (4oz cu) with Buried via (L2- L9) and PTH (L1- L10)



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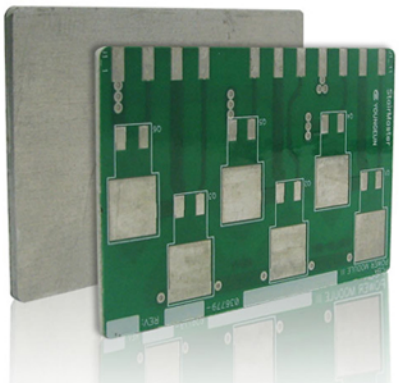

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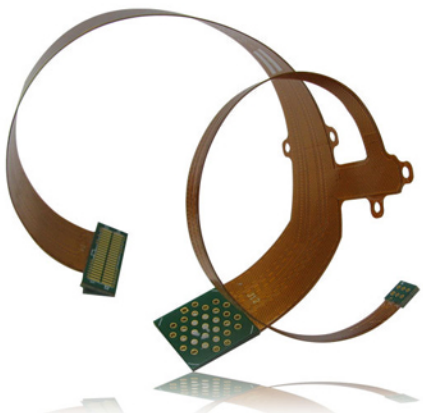

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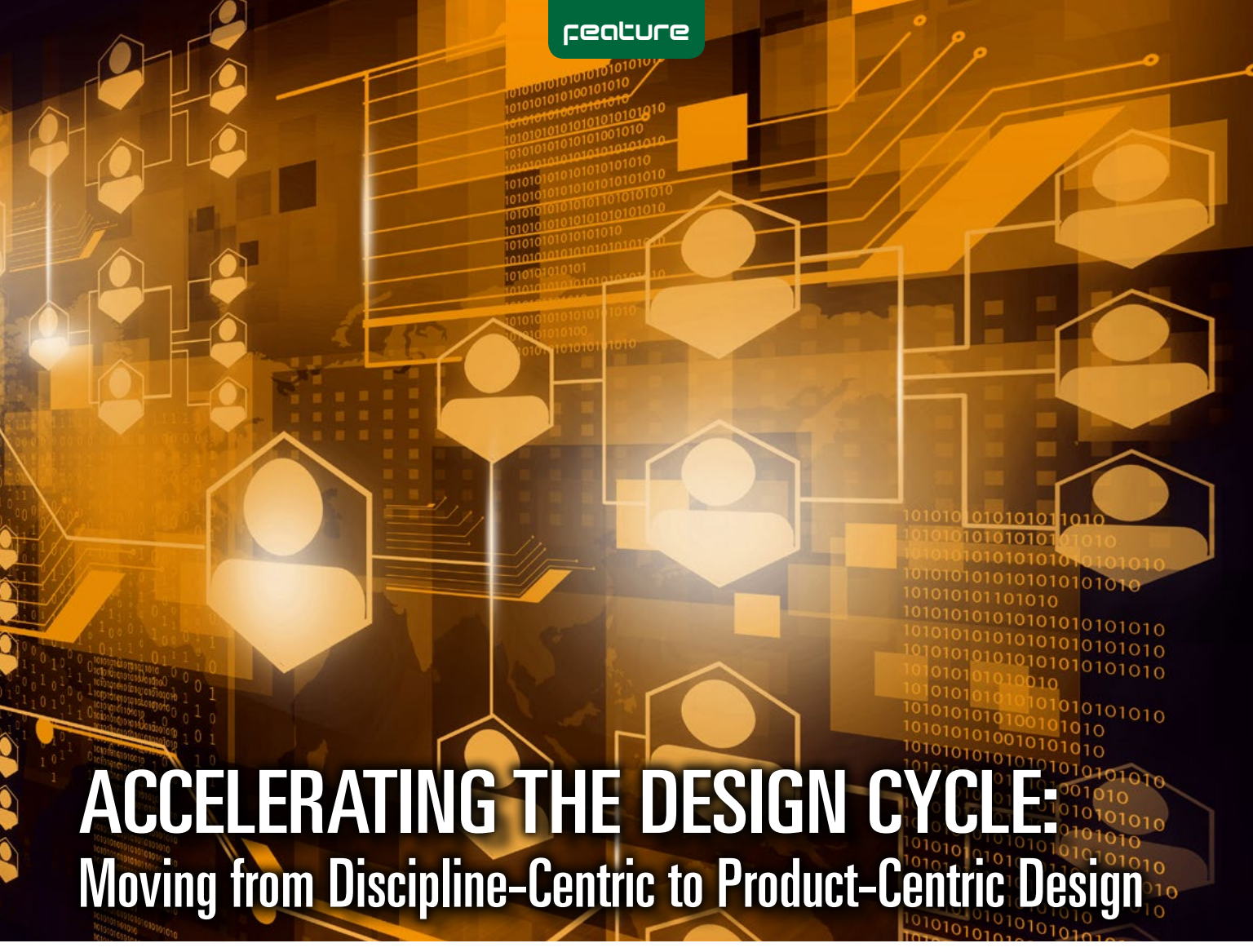

ACCELERATING THE DESIGN CYCLE:
Moving from Discipline-Centric to Product-Centric Design

by Bob Potock
ZUKEN

Defining the characteristics of a new product, such as features, size, weight, and battery life, is the job of marketing. Realizing those design requirements is the responsibility of a multidisciplinary team consisting of product architects, hardware engineers, software engineers, mechanical engineers, packaging engineering, manufacturing engineers, purchasers, etc.

Today, the design process in most cases fans out from the requirements as defined by marketing into multiple independent design threads that converge at the prototype (Figure 1). There is usually no systematic method for these different disciplines to communicate their work to the other disciplines. This lack of communication often leads to conflicting design decisions, such as when an electrical engineer or purchaser selects a component without having any way of knowing that it interferes with the enclosure. Extra design turns are often needed to resolve these conflicts at the prototype stage.

This obstacle, and many others, can be overcome by a product-centric design process that enables all disciplines to work collaboratively during a new virtual prototyping and detailed design. During the architectural validation or virtual prototyping phase, each contributor can optimize the design from their own perspective with visibility and change notices from the others. The product optimization completed during the virtual prototyping process seamlessly transitions to detailed design, preserving all the critical decisions without data loss or re-entry. Product-centric design ensures that the evolving design meets the requirements of every discipline, reducing late stage design changes and enabling the product to be optimized to a higher degree than is possible with current methods.

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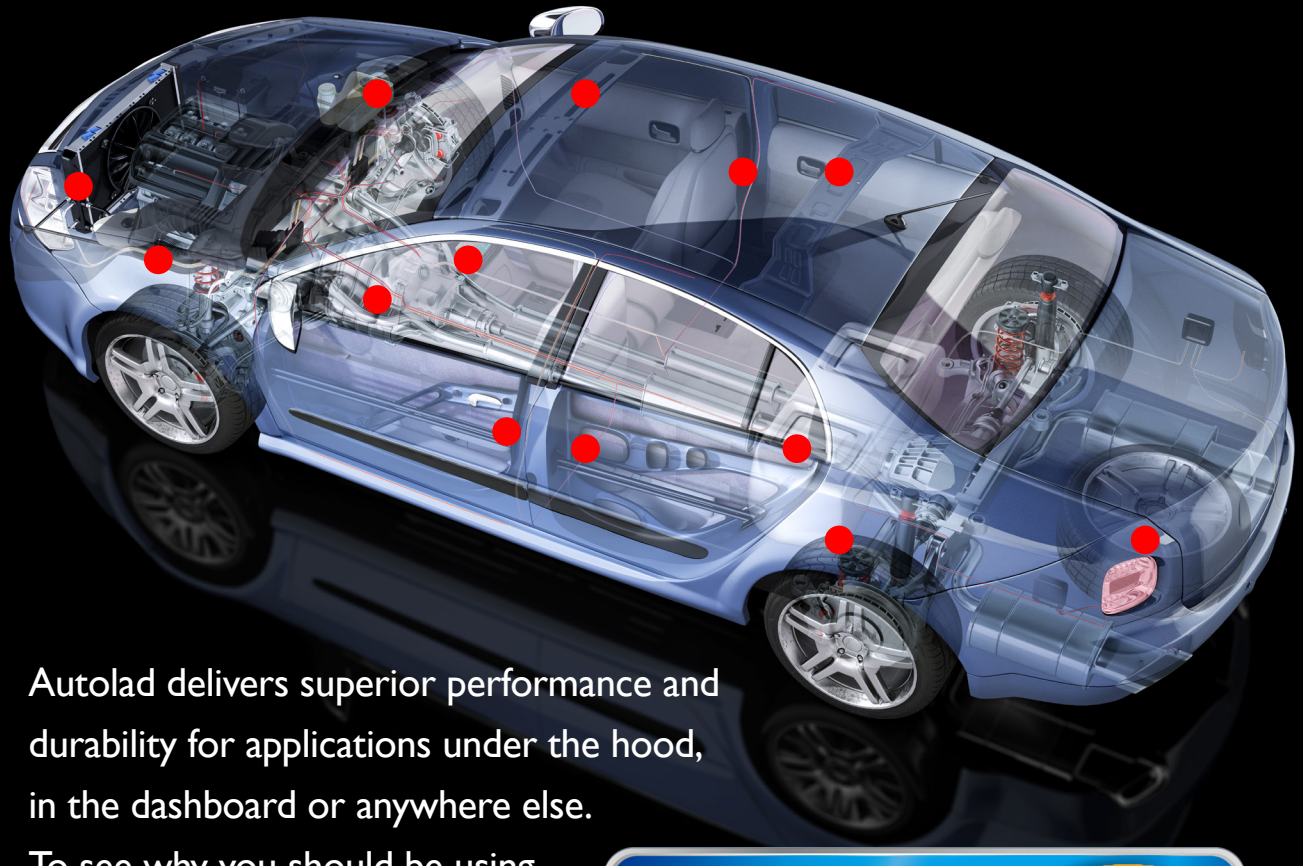

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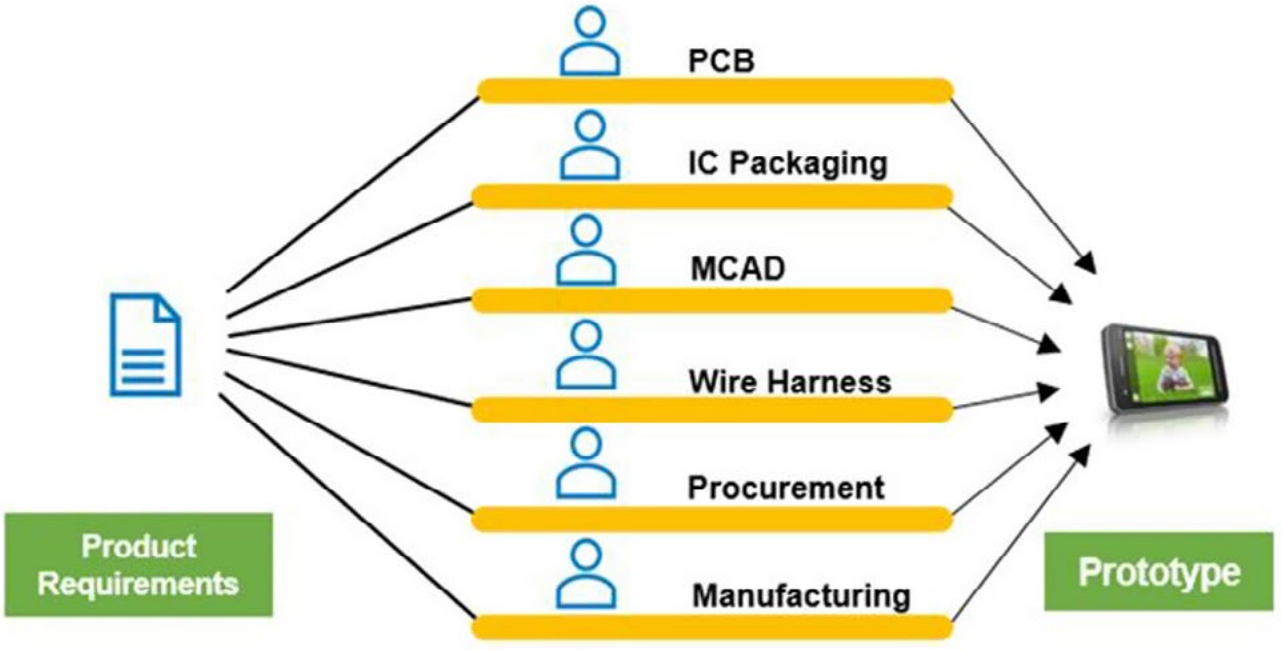

Figure 1: The multidiscipline design process.

Limitations of the Discipline-Centric Process

Looking back just a few years, developers of electronic products primarily competed based on the functionality of their design as determined by unique hardware and software features. Today, with much of the key functionality of electronic products having been commoditized in system-on-chips (SoCs) or application processors, electronics companies are now competing across a wide range of fronts: size, weight, style, battery life and features. The result is a greater need than ever for collaboration across the multiple disciplines that are responsible for providing this much broader range of attributes. More than ever before, a multidiscipline collaborative effort is required to deliver the best design that conforms to marketing requirements in the shortest possible time and at the lowest possible cost.

Yet the tools used to support product development and the process itself have not yet evolved to this new reality. In most cases, the marketing department draws up the requirements documents that then explode into multiple independent paths. The creative team styles the product. The procurement team looks at part cost. PCB designers design the boards one at a time. The manufacturing team decides where to make the product and what processes to use. Mechanical engineers design the enclosure. There may be some limited informal collaboration between disciplines using a spreadsheet or flowcharting tool prior to detailed design, but for the most part, each of these disciplines works independently with relatively little interaction with the others. This is a critical time where architectural decisions are being made with very little validation. In addition, this is generally a sidebar process whose results are not easy to integrate back into the separate design disciplines or into the detailed design; any communications errors can be disastrous.

The very nature of multi-discipline design processes suggests that decisions are frequently made that are good for the discipline that made the decision but detrimental to the overall product. For example, the PCB designer might decide to relocate a connector on the bottom right side of the PCB because it is beneficial from a signal integrity standpoint. But when the industrial designers become aware of this decision they might object because users tend to rest their fingers in this location. And the mechanical engineers may conclude that having an additional

opening in this area will cause excessive stress levels in the enclosure.

Or marketing might specify a compact enclosure, a wide range of electrical features and a long battery life. Electrical designers may be well along in the design process before they are informed by the mechanical engineering team that there is no room for a battery with sufficient capacity to meet the spec.

Another limitation of current design methods is that traditional 2D PCB design systems are used to design one PCB at a time in isolation from the other PCBs within a product, and also in isolation from the enclosure. Verifying board-to-board connectivity in today's 2D PCB tools is a manual process, and one that is prone to error. When mechanical engineers don't have precise information on the electrical design or electrical engineers have inaccurate information on the mechanical design the result frequently is that connectors don't mate with package openings, components interfere with the enclosure, etc. Using current design methods, problems that cross the electrical-mechanical divide often are not identified until the prototype stage, at which point they are expensive and time-consuming to resolve.

Another disconnected aspect of the traditional design process is that the chip, package and PCB are typically designed with three independent design processes, carried out with point tools where data interchange requires time-consuming manual processes. In the past, this approach was acceptable due to lack of alternatives, and because most electronic products had large form factors making package optimization less critical. With increasing functionality, tighter cost constraints, and the decreasing form factor of today's products, the need for vertical integration of chip, package and board is becoming more mainstream. This is particularly true for the growing proportion of products utilizing complex new packaging solutions such as package-on-package (PoP) and system in package (SiP). These new technologies, combined with the increasing functionality of single package modules, create vast new challenges for package designers and the IC and PCB designers who must integrate the package into their own work.

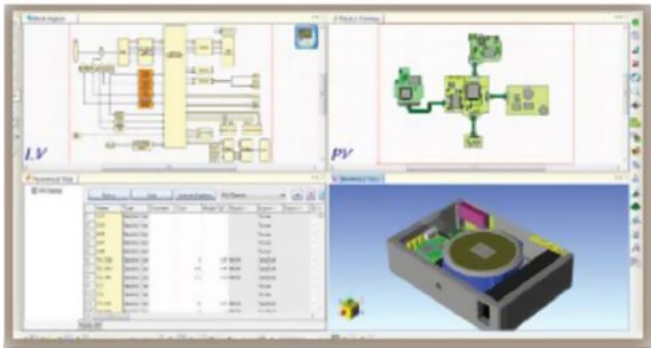

Figure 2: Product-based virtual prototyping.

Moving to a Product-Centric Design Process

The basic idea behind a product-centric design methodology is to optimize and validate product architecture prior to moving into a collaborative 3D detailed design process with product visualization. Product-centric design begins with a product-based virtual prototyping step bridging requirements definition and detailed design using a design tool that integrates product level bill of materials (BOM), functional design, PCB planning and space planning. During this phase, architectural decisions can be made that involve cost, number/size of PCBs, PCB orientation, weight, enclosure size, battery size, and more. Important decisions can be evaluated collaboratively with the ability to make trade-offs before committing to detailed design. Any design change in one planning discipline is immediately propagated to the others with a change notice. The design change can be accepted, or if questionable, can drive a design discussion for resolution.

The functional design can be created using an existing detailed design, BOM-based functional blocks or reuse blocks in order to speed up the design process. Users can also incorporate reference designs provided by SoC manufacturers. The product-level BOM supporting multiple boards is immediately available and can be evaluated by procurement or manufacturing. The functional design is immediately available for PCB planning.

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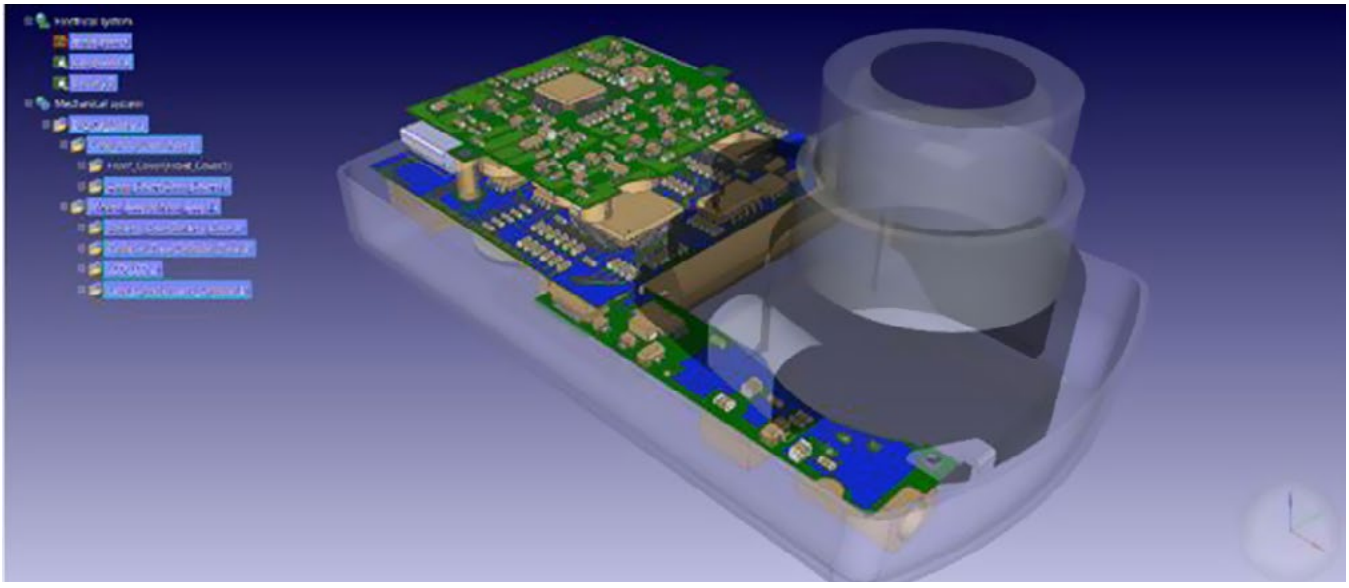

Figure 3: 3D multi-board design promotes electrical-mechanical collaboration.

A key aspect of the new generation of product-centric design tools is their ability to manage a multi-board design as a 3D system in the context of the enclosure as well as the complete mechanical design. During PCB planning designers can manage all of the boards in the system in a single view and evaluate the trade-offs involved in changing the number, size, type and configuration of PCBs while moving functions between them. Changing a board size will propagate to the space planning view where the enclosure and the multiple boards can be viewed concurrently with collision checking. Once the architecture is approved, the functional design moves to the schematic authorizing tool, the PCBs move to the 3D multi-board design tool, and data are moved with the push of a button without data loss or re-entry.

During detailed design PCB designers can import the mechanical enclosure via STEP directly into the 3D multi-board design tool in order to get the design right the first time. Electrical designers can thus design to the true 3D constraints as defined by the mechanical engineers while mechanical engineers in turn have access to the true 3D board design exported via STEP. Design checks for collisions and clearance are done throughout the design process eliminating any late design cycle surprises.

System-level 3D co-design tools enable co-design of the chip, package and board in a single environment so each person working on the project can see their piece of the puzzle in context of the full product. Engineers can do system-level design, full package design, full PCB design, interposer design, and optimize the redistribution layer (RDL) routing and die bump placement for IC design in a single user interface. The mechanical enclosure design can be checked against the final ECAD form factor (PCBs, packages, and ICs) dimensions to ensure fit and clearance. An integrated design-for-manufacturing tool makes it possible to verify the design to vendor technology-specific manufacturing checks for fabrication and assembly during layout. Push button integration with multi-physics analysis tools ensure design data is transferred efficiently and quickly to achieve quick turnaround.

Conclusion

With industry-leading products now competing on a wide range of parameters such as features, weight, performance, size, style and battery life, designing competitive products requires a more collaborative effort now than ever before. A new product-centric design methodology provides a holistic view of the design that enables complete visibility to all disciplines

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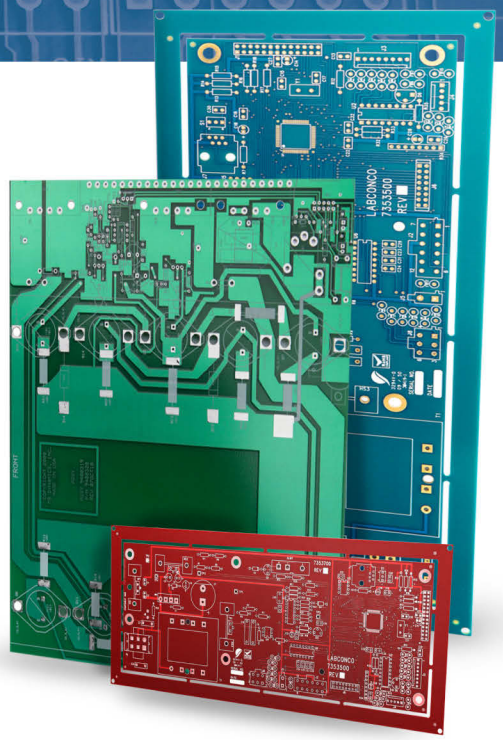

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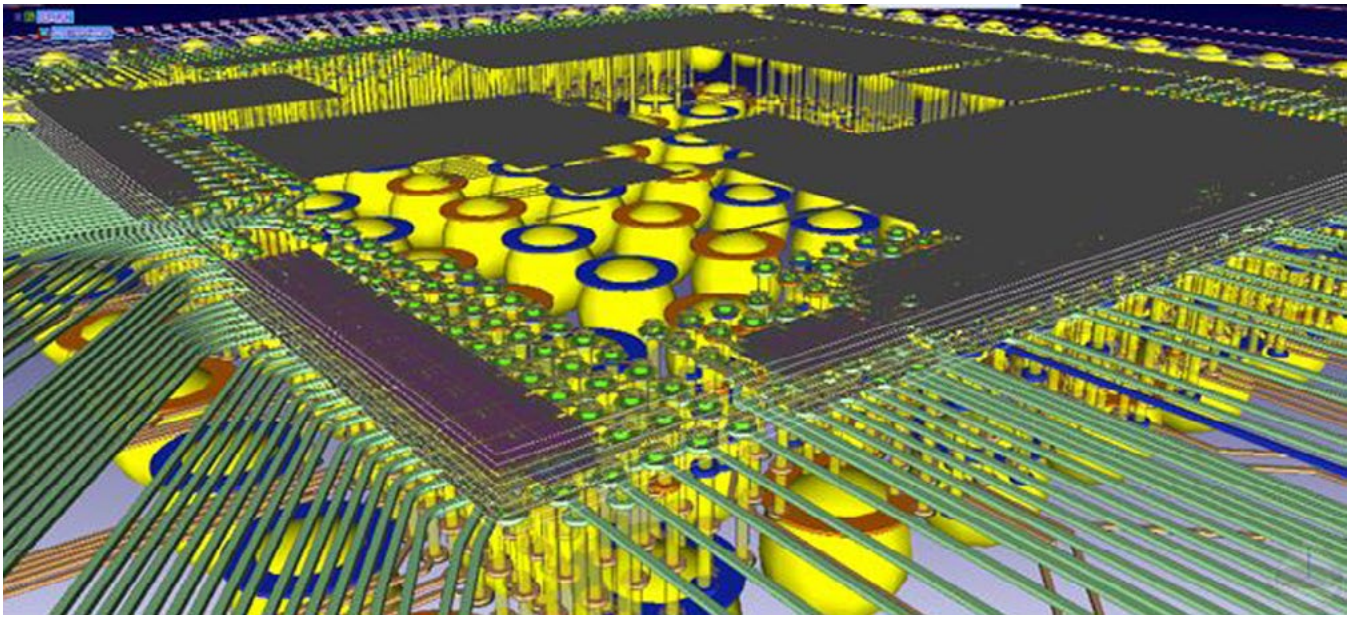


Figure 4: Unified PCB and IC packaging.

involved in the design process so the product can be optimized before committing to detailed design. Product-centric design tools manage multi-board placement in both 2D and 3D while enabling co-design of the chip, package and board in a single environment. Transforming electronic product design from a series of silos to a multidisciplinary collaborative process accelerates time-to-market by reducing the number of design turns required and increases product quality by enabling better design decisions. **PCBDESIGN**

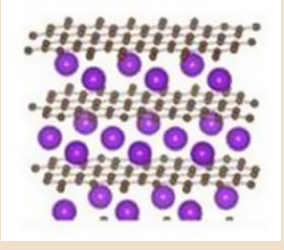
Bob Potock brings more than 20 years of marketing and product management experience in the EDA industry. He has held positions in engineering, product management and marketing at companies that include Altium, Mentor Graphics, AT&T Bell Labs, Intel and Burroughs. Prior to joining Zuken, Bob was vice president of marketing for Kozio Inc.

Discovery about New Battery Overturns Decades of False Assumptions

New findings at Oregon State University has shown that potassium can work with graphite in a potassium-ion battery.

"For decades, people have assumed that potassium couldn't work with graphite or other bulk carbon anodes in a battery," said Xiulei (David) Ji, the lead author of the study and an assistant professor of chemistry in the College of Science at Oregon State University.

The Journal of the American Chemical Society published the findings from this discovery, which was supported by the U.S. Department of Energy and done in collaboration with OSU researchers Zelang Jian and Wei Luo.



That alternative to lithium, he said, may be potassium, which is 880 times more abundant in the Earth's crust than lithium.

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- Relationship management skills and openness to feedback
- Experience in the electronics industry desirable

Successful candidates should possess a BS/BA degree or equivalent and have experience with systems-based management/TQM philosophy. This is a base salary-plus-commission position. Compensation commensurate with experience.

Qualified candidates should submit resumes here.

I-Connect007
GOOD FOR THE INDUSTRY

THE READERS SPEAK:

Tips on Accelerating Your Design Cycle

by Andy Shaughnessy
I-CONNECT007

This month, in addition to publishing feature articles by well-known experts in the field, we decided to collect feedback from the readers—PCB designers and engineers working in the trenches each day. We asked our readers to provide their favorite tips, tricks, and techniques for speeding up the PCB design cycle. Here are 10 tips for cutting your design time, courtesy of designers just like you.

Matija Milostnik
PCB group leader, Slovenia

"Bang on the electrical engineers to squeeze out of them all constraint upfront before starting a design, so that you can put them into rules in the design tool, and then hold them accountable for changes. The rest is easy, in comparison."

Barry Olney
Managing director,
In-Circuit Design Pty Ltd.,
Australia

"Perform pre-layout analysis to ensure your design is right the first time without costly iterations. Having the project completed on time, and within budget, means that costs are cut by reducing the design cycle and generating higher profits due to shorter time to market and an extended product life cycle."

Santiago Cervantes
CID+, San Diego

"Know the system the PCB integrates into."

Karl Bates
President of ConnectPCB, Chicago

"Use both hands (i.e., one hand on the mouse, other using shortcut keys or function keys). Type without looking at your hands (they should know where the keys are)."

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THE READERS SPEAK: TIPS ON ACCELERATING YOUR DESIGN CYCLE

Scott McCurdy
Director of sales and marketing, Freedom CAD Services

"Invest in script automation. Most CAD systems have a macro script language that allows you to automate functions and greatly increase your productivity, such as dalTools for Allegro."

Jens Hansen
PCB designer, Aalborg, Denmark

"Learn the limitations of the PCB fabrication process and set up your PCB CAD system accordingly."

Felipe Lopez Rendon
Packaging design engineer with Intel, Guadalajara, Mexico

"Keep the DRC on most of the time."

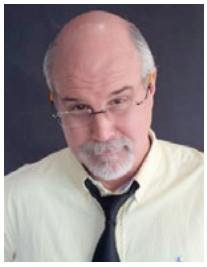
Jean Bratton
Senior PCB designer, Freedom CAD Services

"For anything you need to type/do more than a couple of times, set up a function key, script, or whatever so that it's just a button push."

Anton Erasmus
Electronic engineer, M-TEK (Pty) Ltd., South Africa

"Check netlists for missing nets, and autoroute any PCB with ridiculously small tracks, clearances, and via sizes. Also, autoroute with however number of layers one requires to 100% route the PCB. Then enable only the top layer, and zoom in. Check every surface mount pad to see if it is connected by a track. If no track is connected to an SMT pad, then verify on the schematic whether it should be unconnected. Repeat for the bottom layer. On a PCB that uses mostly SMT components, this is a very quick way to find all sorts of errors in schematics, which cause incorrect routing of signals."

Kelly Dack
PCB designer, EMS company, Eastern Washington state



"I always try to start the design with the end in sight. This involves proactive collection and consideration of all design constraints before the CAD layout tool is ever launched. Identify all of the 'design fors' that may apply: design for test (DFT); design for cost (DFC); design for manufacturability (DFM), and design for all (DFx). Meeting with each respective stakeholder in the design and manufacturing process is key to making sure that expectations can be sufficiently met. Constraints must be weighed for compromise. When things begin to get tight during the layout phase, I want to be in the position of having enough information to intelligently justify robbing Peter to pay Paul. More communication up front prevents slowdowns later!

We hope these tips are useful. What are your favorite time-saving design tips? Let us know! Click here. **PCBDESIGN**

Superconductivity Trained to Promote Magnetization

Superconductivity, which is almost incompatible with magnetic fields, under certain conditions is able to promote magnetization. Russian scientist Natalya Pugach from the Skobeltsyn Institute of Nuclear Physics at the Lomonosov Moscow State University discovered this effect with her British colleagues, whose theory group is headed by Professor Matthias Eschrig. They suggest that techniques based on this effect are able to move us closer to future supercomputers: spintronic devices.

The research team studied the interactions between superconductivity and magnetization. The results of this new research show, that superconductors may be useful in the process of spin transportation, and ferromagnetics may be used to control spins. It is quite possible that the finding will allow development of conceptually new spintronic elements.

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PCB007 Highlights

Characterization of PCB Material & Manufacturing Technology for High-Frequency

Concepts like Industry 4.0, Internet of Things, M2M communication, smart homes and communication in, or to cars are maturing. All these applications are based on the same demanding requirement—a considerable amount of data and increased data transfer rate. These arguments present major challenges to PCB design and manufacturing.

Automotive Technology: The Next Driving Force in Electronic Manufacturing

The devices we have come to expect in luxury and high-end vehicles are now becoming available and even common in lower priced ones. While that significantly increases automotive electronic device manufacture volume, the next wave will dwarf what we have experienced to date.

Conflict Minerals Study: Only 25% of Filers Fully Met Dodd-Frank Section 1502 Requirements in 2014

A recent, independent evaluation of the public company "conflict mineral" filings submitted to the SEC for reporting year 2014 under Dodd-Frank Section 1502 found that of the 1,262 companies evaluated, 312 scored a perfect 100% and 245 scored below 75% in meeting the requirements of the SEC rule.

Detroit vs. Silicon Valley: What's Driving the Proliferation of Automotive Electronics?

For the past several decades, modern cars have not changed much. They have four wheels, an engine, a radio (possibly even an 8-track) and seatbelts. Over time, however, cars' electronics parts have evolved faster than any other part of a car with enhancements like power windows, power mirrors, seat heaters and GPS navigation.

Lone Star Circuits Adds Lance Riley as VP of Sales

Lone Star Circuits, a high-reliability technology driven printed circuit board manufacturer, is pleased to announce that Lance Riley has joined the company as Vice President of Sales.

Flex Market Evolution

Flex circuits are designed to solve electronic packaging and assembly problems, solve interconnection issues, assist in miniaturization, and provide a dynamic electro-mechanical solution. They are configured with repeatable conductors that foolproof assembly errors. Flex is used in designs where standard PCBs, connectors and cable assemblies just don't provide the right electrical or mechanical solution.

Georgia Tech Joins Manufacturing Innovation Institute for Flexible Hybrid Electronics

The Georgia Institute of Technology has become a founding member of the new Flexible Hybrid Electronics Manufacturing Innovation Institute (FHE-MII) established by the U.S. Department of Defense.

IPC Releases White Paper on Conflict Minerals Due Diligence

The Dodd-Frank Act continues to be burdensome for companies required to report on the usage of conflict minerals. In order to address industry concerns, IPC–Association Connecting Electronics Industries has released IPC-1081, Conflict Minerals Due Diligence White Paper (IPC WP-1081), a document designed to help with some reporting woes.

Integrating with Gardien Group's Roland Valentini

Gardien Group is one of those companies that are always looking out for their customers. The company is, without a doubt, the last word when it comes to bare board quality assurance, focused on helping customers deliver the most electrically sound boards in the business. Gardien's technologists are experts at testing and other quality assurance disciplines.

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Speeding up the Design Cycle: 10 Things to Remember

by Mark Thompson
PROTOTRON CIRCUITS

Many people understand the value of a PCB, but do not understand the best way to interact with PCB manufacturers. Poor planning and communication with fabricators slows down the design cycle and increases overall costs for your project.

In this column, I will attempt to help streamline the design cycle through fabrication. Following my tips will minimize the need for future revisions and ensure you get quality boards on time.

10. Eliminate Conflicting Information

It is essential that you eliminate any conflicting information from your drawings or read-me files. Make sure that all documentation is the same. If one document says half-ounce and another says one-ounce copper, you may expect a call asking which it is to be. If you need the part expedited, remember that this takes valuable time away from the build and from you getting your part.

9. Provide an IPC Netlist

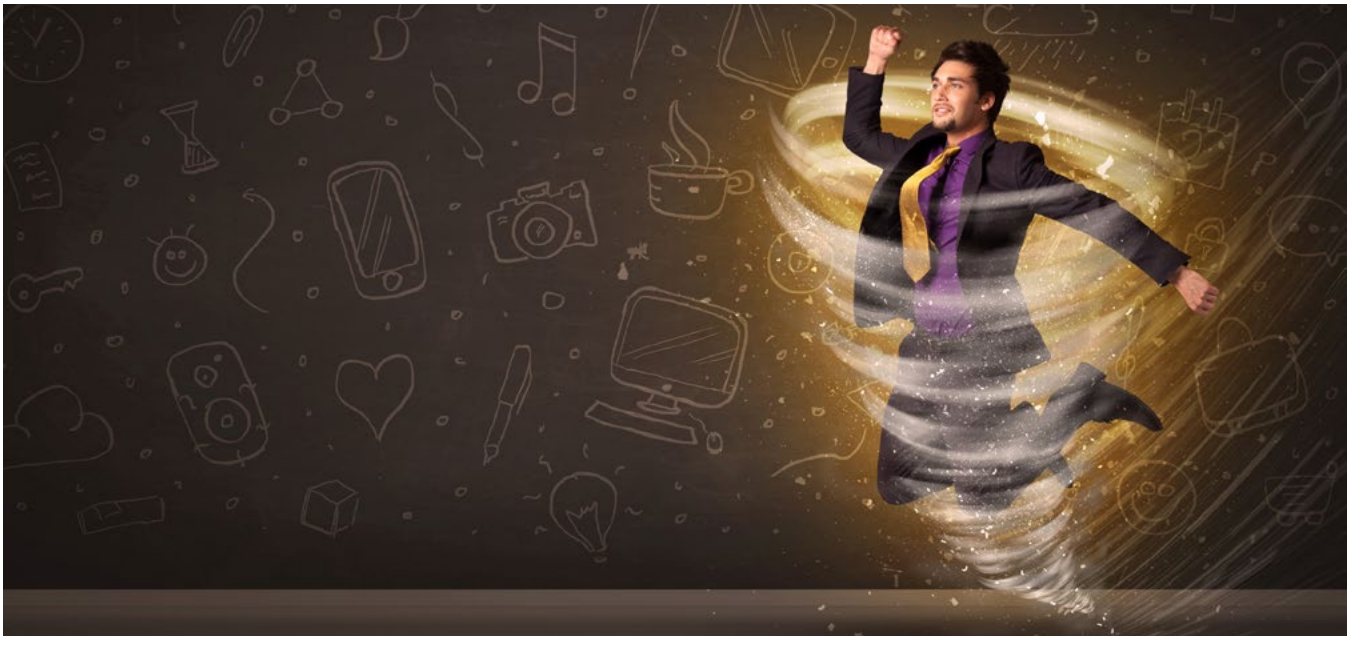
An IPC netlist will allow the fabricator to check your design against your exported data. Make sure any known or intentional netlist mismatches are noted again so your CAM group does not waste time calling you to check on things you are already aware of.

Be careful with castellated pads where plated half-holes at the board's edge will make a connection to a post at some point after fabrication. These typically come up as "broken" or open nets because when the bare boards are fabricated, no post exists to connect these castellations.

Known A-gnd to D-gnd shorts should also be noted. Make sure no non-plated holes have been specified as test points on the IPC netlist. If you are specifying net-compare on your documentation, be sure to include it!

8. Check for Discrepancies on NC Drill File

Double-check to ensure there are no discrepancies of count, size or plating status on the NC



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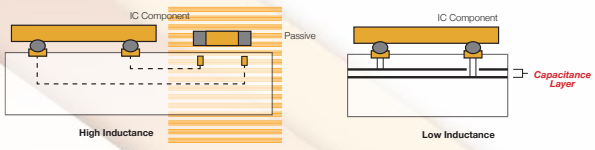

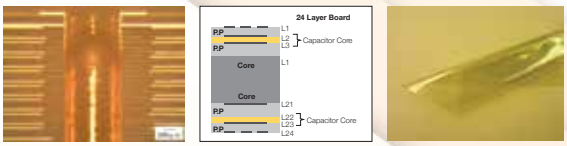

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drill file. Either one of these can cause communication delays.

7. Communicate With Your Fabricator ASAP

In order to facilitate the best communication, you need to meet with your chosen fabricator as soon as possible in the design cycle. Check with them for validation of any impedance you may have. Make sure these notes do not conflict either.

Be sure to: Check for proper reference planes. Make sure impedance traces do not traverse multiple splits or lack ref-planes altogether. Differentiate between single-ended and differential type structures by a tenth or a hundredth of a mil. Again, fabricators cannot resolve these small increments, but this allows the fabricator

"In order to facilitate the best communication, you need to meet with your chosen fabricator as soon as possible in the design cycle."

to uniquely select just the impedance tracks for any resizing that may be necessary to meet desired impedances.

Make sure the space between differential pairs is consistent throughout the run. Allow for process deviation, setting up a part as .1 mm trace and space on half-ounce starting copper does not leave room for any trace resizing that may be necessary to meet the impedances if dielectric cannot be altered.

When calling out materials, call out the 4101/# such as 4101/126. This will allow the fabricator to use any material that falls within the /126 criteria. Calling out a specific material may limit the pool of fabricators that can build the board. Avoid creating same net spacing violations when terminating differential pairs, and do not "wrap" the differential pairs around the terminus.

6. Annular Ring must be Adequate and Communicated in Plans

Make sure all pads for plated through-holes have sufficient annular ring. The general rule of thumb is .010" MIN larger than the FHS (finished hole size) for signals and .015" MIN for internal relief/antipads. For vias, you may want to specify +.003" /- the entire hole size. This tells the fabricator in no uncertain terms they are indeed vias and can be drilled smaller if necessary.

5. Check Your Edges

For scored parts, do not pour metal any closer to the part edge than .015" for an .062" board, and at least .009" for an .031" thick part.

4. Check Your Drill Aspect Ratio

If your drill aspect ratio is greater than 10:1, be sure to consult your chosen fabricator.

3. Communicate Uncommon Materials

If using an uncommon material type, make sure you call the chosen fabricator to make sure it is something they stock or can get quickly.

2. File Naming

When exporting Image files avoid the use of control characters in the file names. And finally, the Number 1 thing to remember to help you streamline your design through fab process:

1. Consult Your Fabricator

Be sure to consult your fabricator and discuss any deviations you may require. Be specific about any special needs for the part, such as extremely tight tolerances or additional edits necessary. This is the key to accelerating your design process. **PCBDESIGN**

Mark Thompson is in engineering support at Prototron Circuits. His column, *The Bare (Board) Truth,* appears bimonthly in *The PCB Design Magazine.* To read past columns, or to contact Thompson, click here, or phone 425-823-7000, ext. 239.

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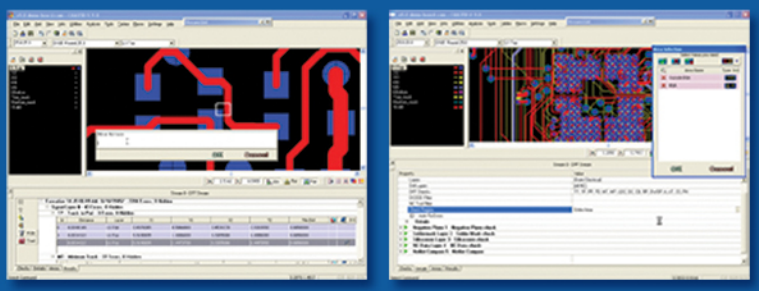

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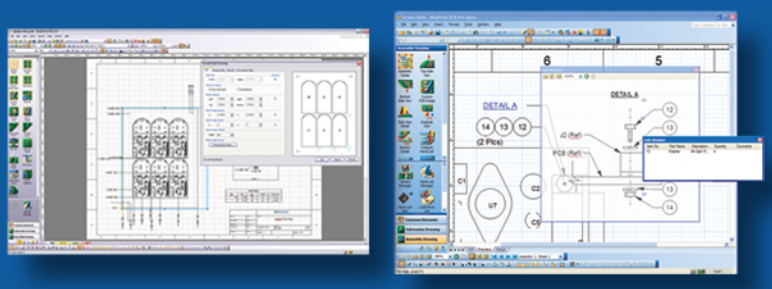

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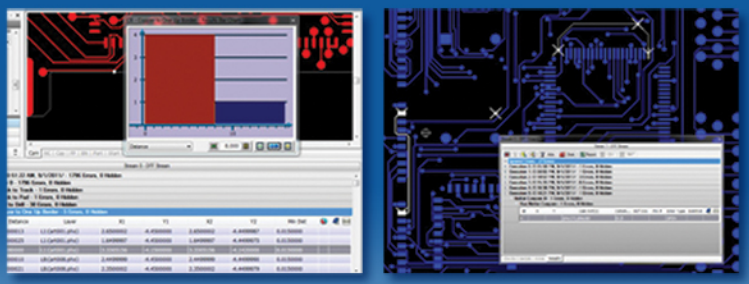

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Stackup Planning, Part 4

by Barry Olney
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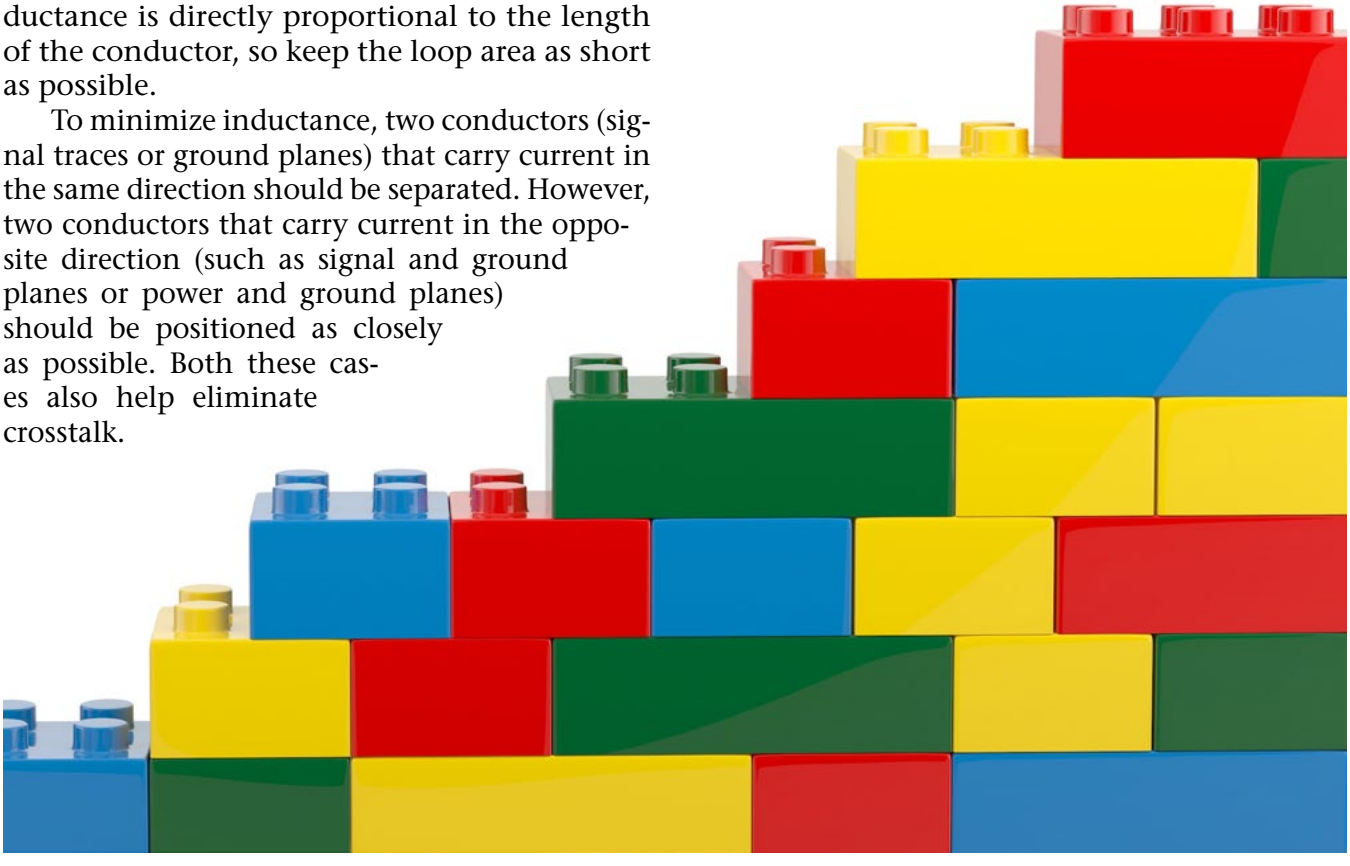
In the final part of the Stackup Planning series, I will look at 10-plus layer counts. The methodology I have set out in previous columns can be used to construct higher layer-count boards. In general, these boards contain more planes and therefore the issues associated with split power planes can usually be avoided. Also, 10-plus layers require very thin dielectrics, in order to reduce the total board thickness. This naturally provides tight coupling between adjacent signal and plane layers reducing crosstalk and electromagnetic emissions.

In high-speed digital designs, transient ground currents are the primary source of both unwanted noise voltages and radiated emissions. In order to minimize these emissions, the impedance of the ground should be minimized by reducing the inductive loop area. Inductance is directly proportional to the length of the conductor, so keep the loop area as short as possible.

To minimize inductance, two conductors (signal traces or ground planes) that carry current in the same direction should be separated. However, two conductors that carry current in the opposite direction (such as signal and ground planes or power and ground planes) should be positioned as closely as possible. Both these cases also help eliminate crosstalk.

Here are some additional rules for high-speed design:

1. Use multiple ground planes, where possible, rather than power planes, in the stackup to isolate signal layers.
2. Place stitching ground vias close to every signal transition (via) to provide a short current return path.
3. Spread numerous ground stitching vias around the board to connect the multiple ground planes through a low impedance path.
4. Don't use ground pours on signal layers as this reduces the impedance of nearby traces. If you must, in order to balance copper, separate the signal and pour by 20 mils.



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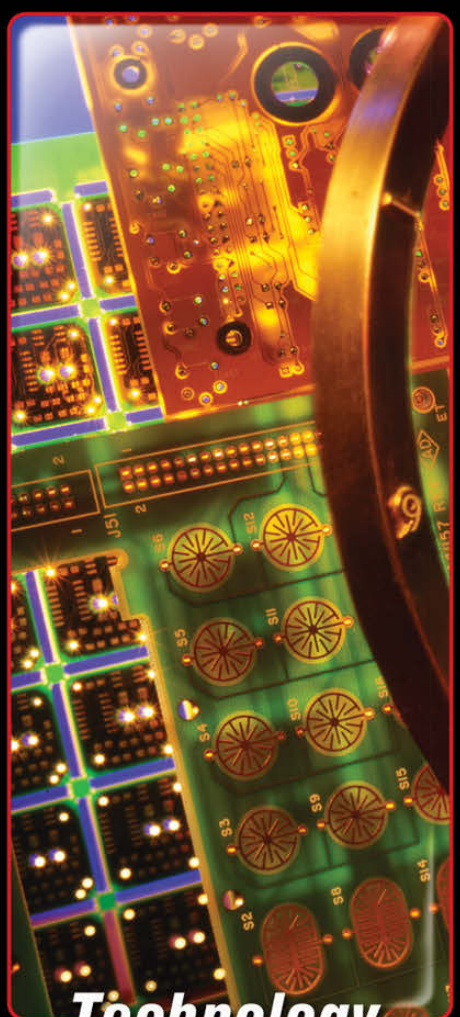

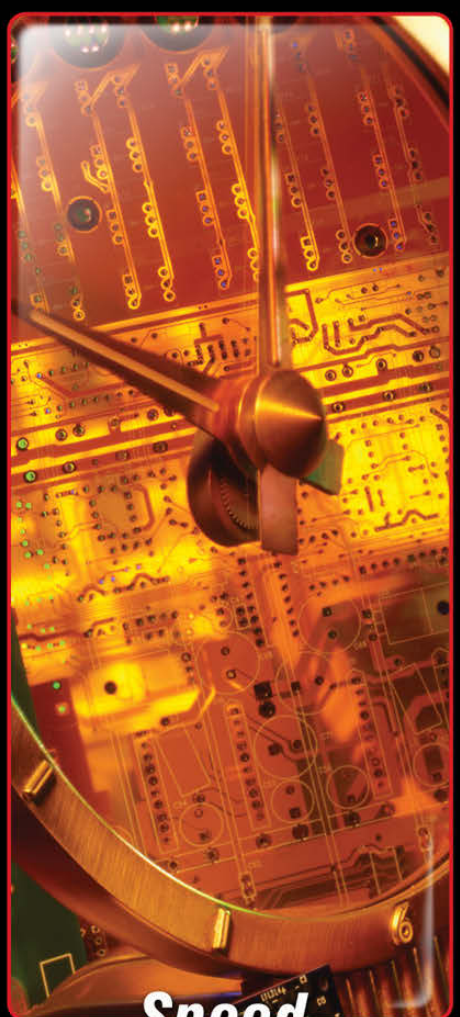

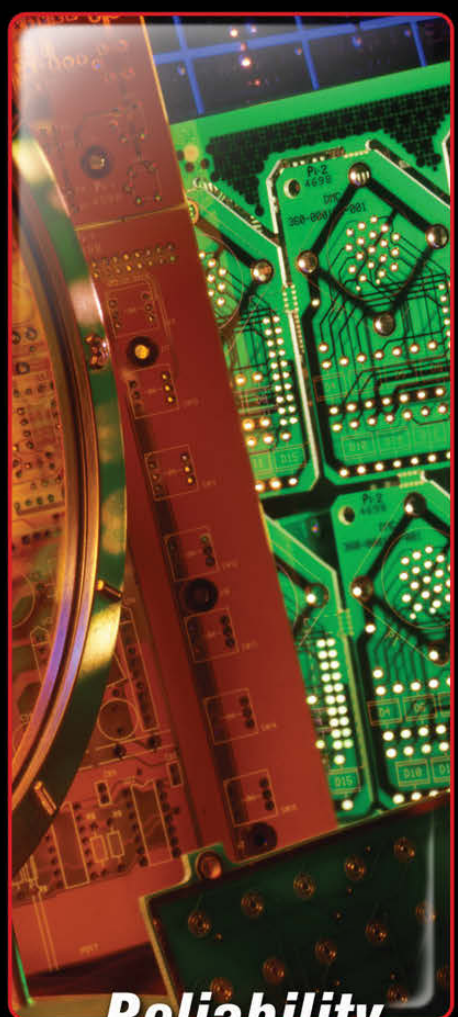

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If power planes are used as reference planes, then the return current must transverse stitching capacitors in order to jump between ground and power planes. The current flowing through these stitching capacitors will create a voltage drop across them. These voltages may radiate adding to system noise problems.

Determining the required layer count: the number one question!

Over the years, a number of people have put forward equations to determine the route density. Rent's Rule is one such model.

$$Trace\ Pitch = \frac{\sqrt{X.Y}}{n} 2.7M$$

where: n is the number of nets
X and Y are the board width and length in inches
M is the number of routing layers

Good luck getting any serious results from such equations. There are just too many variables to take such a basic approach to layer count determination. This is my line of attack:

As with Rent's Rule, I start with the route pitch. Technology rules are based on the minimum pitch of the SMT components employed and are basically the largest trace, clearance and via allowable whilst minimizing PCB fabrication costs. Technology of 4/4 mil (trace/clearance) and vias of 18/8 mil (pad/hole) are generally required for complex high-speed designs incorporating BGAs. However, if you can use less demanding dimensions, then this will reduce cost and improve fabrication yield.

Once these rules have been established, calculate the stackup required for the desired characteristic impedance (Zo) and the differential impedance (Zdiff) as per the component datasheets. Generally, 50/100 ohm Zo/Zdiff are used. Keep in mind that lower impedance will increase the dI/dt and dramatically increase the current drawn (not good for the PDN). While higher impedance will emit more EMI and also make the design more susceptible to outside interference. So, a good range of Zo, for a digital design, is 50–60 ohms.

The total number of layers required for a given design is dependent on the complexity of the design. Factors include:

- The number of signal nets that must break out from a BGA.
- The number of power supplies required by the BGAs.

Differential Pairs > 50/100 Digital | 40/80 DDR3 | 90 USB

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI (1GHz)	3.5	0.5							
1	8 4 4	Signal	Top Layer	Conductive			1.38	10	4.5	0.34	52.11	99.44	
		Prepreg		N4000-13; 106; Rc=75% (2.5GHz)	3.19	2.63							
2		Plane	GND_TOP	Conductive			1.38						
		Core		N4000-13; 1080; Rc=61.2% (2.5GHz)	3.4	3							
3		Signal	MidLayer3	Conductive			1.38	12	4	0.31	52.16	98.69	95.35
		Prepreg		N4000-13; 2116; Rc=55% (2.5GHz)	3.56	5.58							
		Prepreg		N4000-13; 3313; Rc=58% (2.5GHz)	3.50	4.32							
		Prepreg		N4000-13; 2116; Rc=55% (2.5GHz)	3.56	5.58							
4		Signal	MidLayer4	Conductive			1.38	12	4	0.31	52.16	98.69	95.35
		Core		N4000-13; 1080; Rc=61.2% (2.5GHz)	3.4	3							
5		Plane	GND	Conductive			1.38						
		Prepreg		N4000-13; 3313; Rc=58% (2.5GHz)	3.50	4.32							
6		Plane	PWR	Conductive			1.38						
		Core		N4000-13; 1080; Rc=61.2% (2.5GHz)	3.4	3							
7		Signal	MidLayer7	Conductive			1.38	12	4	0.31	52.16	98.69	95.35
		Prepreg		N4000-13; 2116; Rc=55% (2.5GHz)	3.56	5.58							
		Prepreg		N4000-13; 3313; Rc=58% (2.5GHz)	3.50	4.32							
		Prepreg		N4000-13; 2116; Rc=55% (2.5GHz)	3.56	5.58							
8		Signal	MidLayer8	Conductive			1.38	12	4	0.31	52.16	98.69	95.35
		Core		N4000-13; 1080; Rc=61.2% (2.5GHz)	3.4	3							
9		Plane	GND_BOT	Conductive			1.38						
		Prepreg		N4000-13; 106; Rc=75% (2.5GHz)	3.19	2.63							
10		Signal	Bottom Layer	Conductive			1.38	10	4.5	0.34	52.11	99.44	
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI (1GHz)	3.5	0.5							

Figure 1: A 10-layer configuration using Nelco N4000-13 2.5GHz material.

- The component density and package types.
- If there are BGAs of 0.8 mm or less, plated-through-hole (PTH) vias will impede the routing.
- Also, with high layer count boards, the via aspect ratio will increase the diameter of the vias. Via length to hole aspect ratio should be less than 8:1 or the reliability will decline significantly. In this case, a combination of PTH and blind and buried vias may be required.

Experienced PCB designers get a feel for it after a while, but a good way to check if you have enough layers is to autoroute the board. With no tweaking, the autorouter needs to complete at least 85% of the routes to indicate the selected stackup is routable. The performance of the autorouter also impacts on the completion rate. You may have to re-evaluate the placement a couple of times to get the best results. In general, eight layers is a good starting point for DDR type designs. Remember, it is much easier to increase the number of layers than to reduce them, so start with the minimum.

10-Layer Stackup

A 10-layer board is similar to an eight-layer with the addition of two more embedded signal layers.

These are used to increase routability and to add planar capacitance. I have used Nelco N4000-13 2.5GHz material (Figure 1). This is another common high-speed material. The stackup accommodates 50/100 ohm digital, 40/80 ohm DDR3 and 90 ohm USB. Also, I have a combination of PTH and blind and buried vias with appropriate aspect ratios for a total board thickness of 60.82 mils. In this case, internal layers 3, 4, 7 and 8 can be used for the DDR3 routing as three of these layers are referenced to GND whilst the other (layer 7) is referenced to the 1.5V DDR3 PDN (or 1.35V in the case of lower power devices). The layer 7 power plane can have a 1.5V island directly above the DDR3 devices. With a 4.32 mil dielectric between the planes, there is also excellent planar capacitance of about 240 pF/in^2. This will reduce the AC impedance of the DDR3 PDN at frequencies about 1GHz which is required for this type of design.

The outer microstrip layers should not be used for routing—except for fanout. Apart from the fact that outer layers radiate more than internal layers, they also vary considerably in impedance. This is due the uneven plating thickness of the final electrolysis process used to plate the though-hole barrels during fabrication. Blind vias can be used to fanout from the BGA and drop directly to either GND or layer 3. The PTH could be used to transverse the signals to the other layers or alternatively a buried via could be used.

Figure 2 illustrates an alternative of buildup microstrip (outer layers). In this case, layer 1 is only used for fanout to layer 2, GND or Power. But layer 2 can be used for high-speed routing of SERDES or other differential signals. It is closely coupled to the layer 3 (GND plane) and will have constant impedance.

12-Plus Layout Count

I could go on and describe each successive layer count in detail, but I'm sure you get the drift by now. Figure 3 illustrates the signal/plane configuration for 12–18 layers. There are of course, many variations that could be employed depending on the application. The ICD Stackup Planner has default stackups from 2–18

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
		Soldermask		Dielectric	3.3	0.7						
1	8 4 8	Signal	Top	Conductive			2.2	10	5.5	0.55	70.13	121.81
		Prepreg		Dielectric	3.7	3.4						
2		Signal	Inner 2	Conductive			0.6	10	4.5	0.18	53.5	99.23
		Core		Dielectric	3.6	3						
3		Plane	GND	Conductive			0.6					
		Prepreg		Dielectric	3.5	3						
4		Plane	VDD	Conductive			0.6					

Figure 2: Buildup microstrip layers.

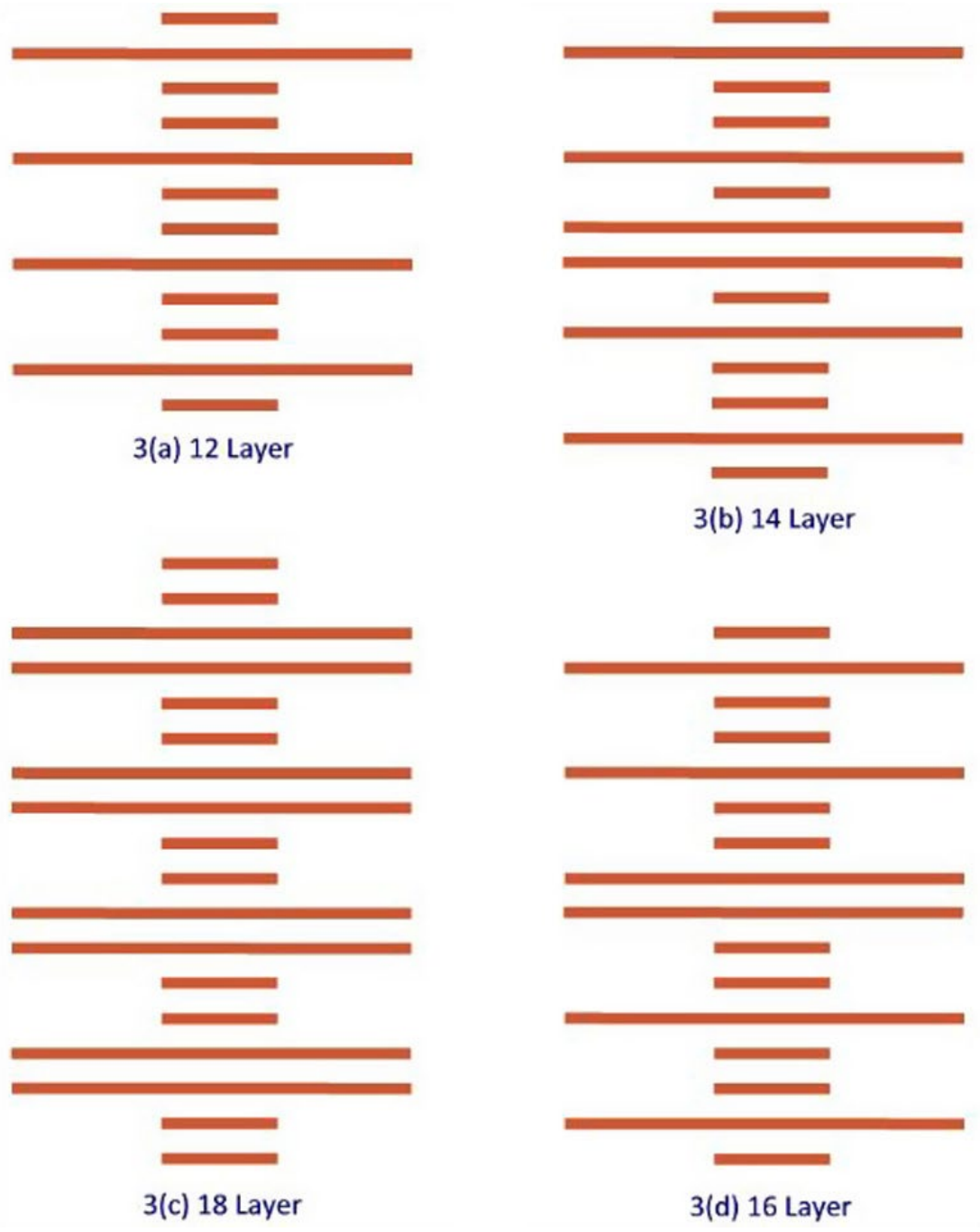

Figure 3: Image illustrating the signal/plane configuration for 12–18 layers.

layers pre-defined to get you started. Figure 3(c), is similar to Lee Ritchey's favorite stackup. This has all the good attributes that I have described, throughout this series, although 18 layers maybe overkill in some cases. But this basic configuration could be cut-down to 14 or 10 layers by removing groups of dual stripline layers.

Be creative. You can use more layers for planes, single or dual stripline routing layers but keep them symmetrical and most importantly, watch the return paths. The layer count always increments by even numbers. So, follow the basic rules I have set out in this stackup planning series and you cannot go wrong. Remember that

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Points to Remember

- To minimize inductance, two conductors (signal traces or ground planes) that carry current in the same direction should be separated.
- Two conductors that carry current in the opposite direction (such as signal and ground planes or power and ground planes) should be positioned as close as possible.
- If power planes are used as reference planes, then the return current must transverse stitching capacitors in order to jump between ground and power planes.
- Use multiple ground planes, where possible, rather than power planes, in the stackup, to isolate signal layers.
- Place stitching ground vias close to every signal transition (via) to provide a short current return path.
- Spread numerous ground stitching vias around the board to connect the multiple ground planes.
- Don't use ground pours on signal layers as this reduces the impedance of nearby traces. If you must, in order to balance copper, separate the signal and pour by 20 mils.
- To determine the layer count, start with the route pitch. Technology rules are based on the minimum pitch of the SMT components employed and are basically the largest trace, clearance and via allowable. Then calculate the stackup required for the desired characteristic and the differential impedances.
- A 10-layer board is similar to an eight layer with the addition of two more embedded signal layers. These are used to increase routability and to add planar capacitance.
- The methodology I have set out, in previous columns, can be used to construct higher layer count boards. **PCBDESIGN**

References

1. Barry Olney Beyond Design columns: Material Selection for SERDES Design, Material Selection for Digital Design, The Perfect Stackup for High-Speed Design, and Embedded Signal Routing.

2. Henry Ott, Electromagnetic Compatibility Engineering.

3. Lee Ritchey, Right First Time Design.

4. Howard Johnson, High-Speed Digital Design.

5. To download the ICD Stackup and PDN Planner, visit www.icd.com.au.

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.

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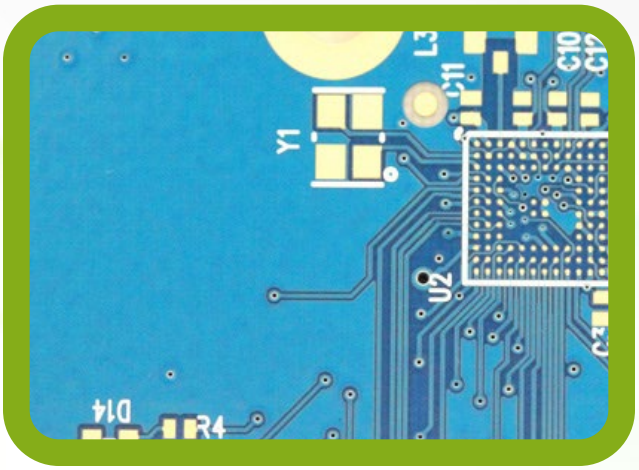

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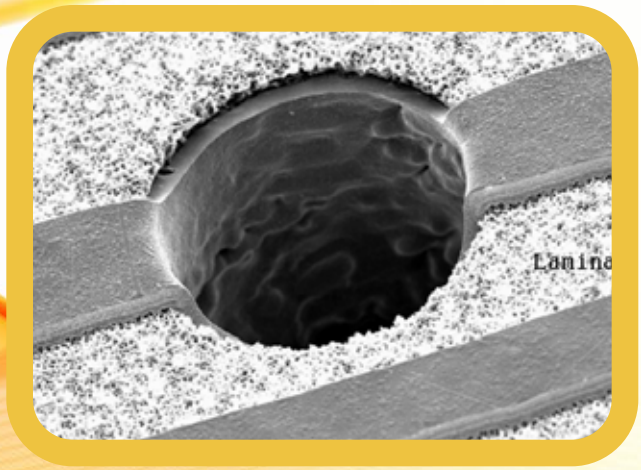

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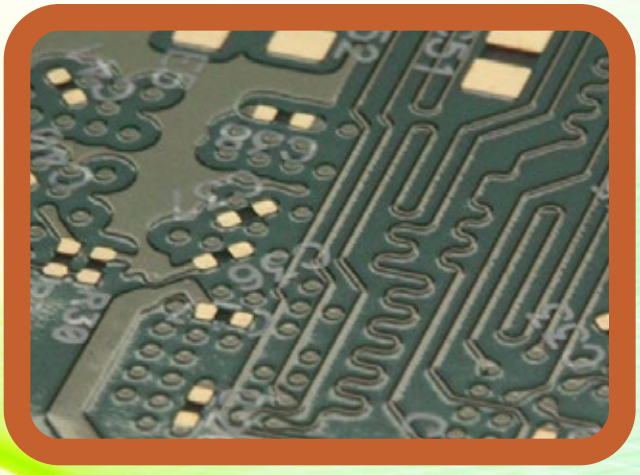

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Avoiding the Black Spot of Negative Expectations

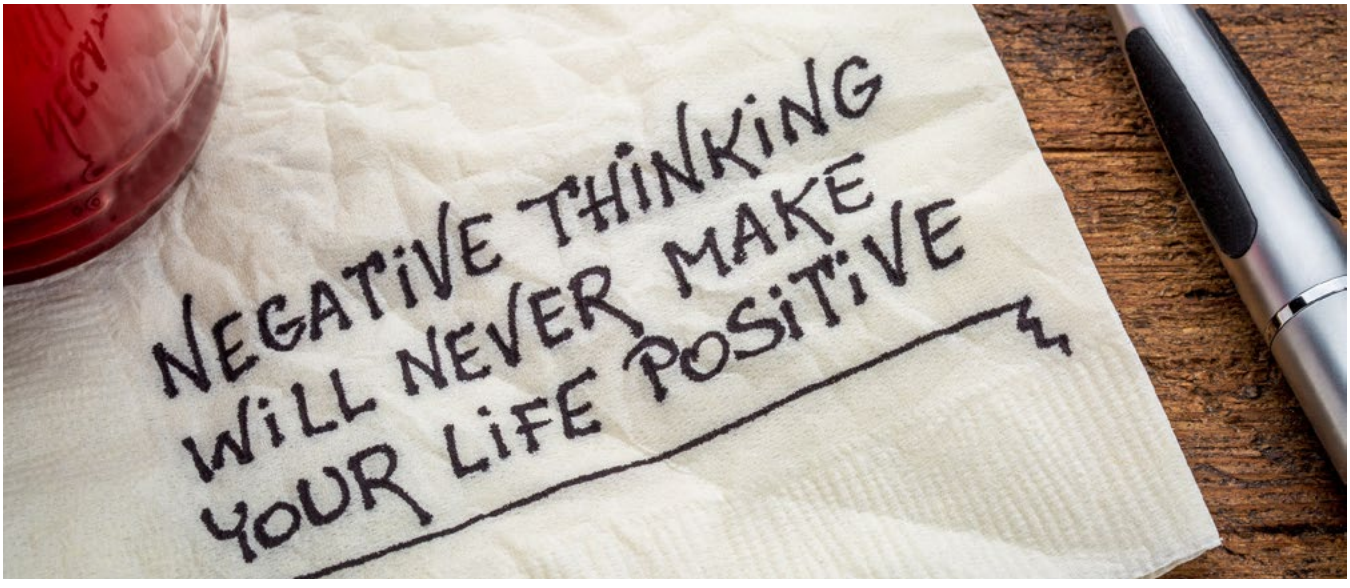
by Tim Haag
INTERCEPT TECHNOLOGY

When I was a boy, our family didn't eat dessert very much, so I wasn't very familiar with different flavors of cake. For me, cake was limited to just two flavors: chocolate and lemon, which I was very content with. But what really puzzled me then was why anyone in the world would eat coffee cake. As a boy, I was disgusted by the bitter flavor of coffee, and therefore, coffee cake seemed to be a food that only an adult would be foolish enough to eat. Since I couldn't stand the taste of coffee, I never tried any coffee cake until years later, and I politely declined whenever it was offered. This preconception that coffee cake should be avoided at all costs stayed with me into my adult life. I didn't realize it, but the notion that coffee cake was evil was buried way down deep.

My wife was confused about this, and finally one day she convinced me to try some coffee cake. "What in the world is this?" I thought at my first bite. Instead of the disgusting assault on my taste buds that I was expecting, I was completely overwhelmed by the sweet cinnamon flavor. I was amazed that for years I had avoided something as wonderful as coffee cake simply because I had expected something bad.

That's a simple and fun example, but negative expectations can also have a dark side. And if not corrected, that negative expectation can potentially be very destructive, especially in a business relationship. Just a few months ago, my wife and I were on vacation and we drove past the restaurant we had visited on our honeymoon. Back then, we waited at our table for our order to be brought to us, but it never came. Three times the waitress came out and told us that they had lost our order and were still looking for it. Finally, after almost an hour without ever receiving our food or even someone offering to re-take our order, we left. And when we drove by that restaurant 30 years later, we had no desire to try our luck again.

This reminds me of Robert Louis Stevenson's "Treasure Island," in which pirates are presented with a black spot on a piece of paper as a sign of guilt or judgement. We were ignored at that



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AVOIDING THE BLACK SPOT OF NEGATIVE EXPECTATIONS

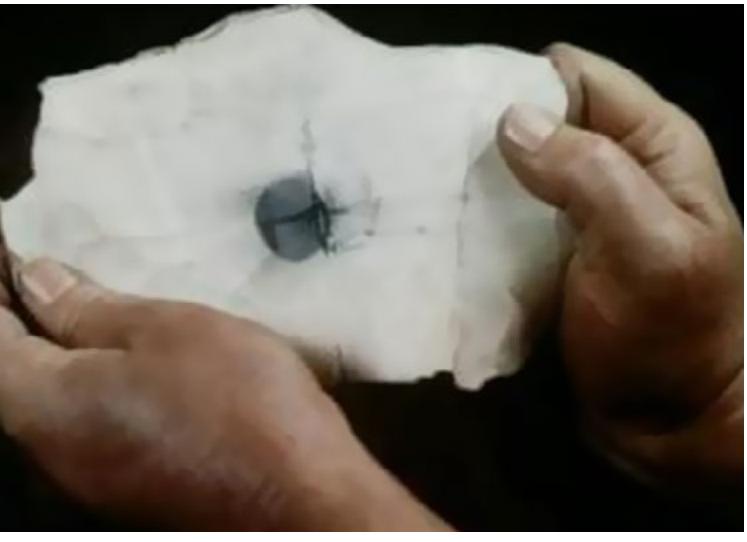


Figure 1: Pirates who were found guilty of various transgressions were presented with a black spot like this.

restaurant 30 years ago, and it resulted in a permanent sense of disgust. We gave that restaurant the black spot and we will never be back.

We all must be careful in our own professional lives to avoid setting negative expectations with our customers and giving them the opportunity to give us a black spot. Since I work in customer support, I see many scenarios that could result in negative expectations and I am constantly working with my staff to identify and minimize those potential problems before they ever happen. It could be something as innocent as missing a support request and leaving a customer stranded with a problem so that they are wary of calling in again. Or it could be the inadvertent presentation of an attitude that projects a sense of indifference to the customer so they feel as if their problems don't matter.

But as I have mentioned before, every work relationship is ultimately customer support. Whether it's your co-worker asking for help with a problem, or your boss assigning you a new task when you are trying to finish what's in front of you, how we treat each of these situations is an extension of our own customer support skills. How we react to these scenarios will ultimately shape our work relationships either negatively or positively. Instead of getting annoyed at the interruptions in our work day, try turning it around to be a positive moment instead; help the co-worker get through the problem and work with your boss to best manage all your tasks. In this way you can avoid the dreaded black spot in the eyes of your co-workers by eliminating any possible negative expectations.

When I was a boy I set a negative expectation for myself that people who flew airplanes were somehow endowed with a greater set of skills and abilities than I could ever achieve. They were pilots after all, something that I could never be. I don't know why I thought that, I just did—I had put a black spot on myself. As an adult I decided to put this to the test and started working on getting my private pilot's license. But all throughout my training was the thought way down deep in the back of my mind that I was trying to do something that was for me unobtainable and therefore a complete waste of time.

This thought continued as I passed my ground school. It continued through my dual pilot instruction and then on through my solos. The day that I took that little airplane to the Hillsboro Airport and picked up my pilot examiner, the thought was still there. Even after successfully passing my practical test and being signed off as a private pilot, the thought was still there. It was only after I was flying back to my home field in Aurora that I suddenly realized that the negative expectation that I had labeled myself with was WRONG. I had given myself a black spot and had allowed that cancerous monkey to ride my back for 20 years. But now, I had beaten it and was an official private pilot. My apologies to anyone listening in to Aurora's Unicom that day; I hope my cries of joy didn't break your eardrums.

How about you? Have you given yourself any black spots of negative expectations that have held you back in life?

I started designing circuit boards more than 30 years ago and my skills grew with each board that I worked on. But the idea of being a high-speed designer seemed to be out of my reach. That, I reasoned, was only for the select few, the elite group of "really good designers" that I did not consider myself part of. Yep, it was the pilot story all over again. Then one day I was as-

signed to do a very complex high-speed board for a computer manufacturer. I was concerned because I didn't consider myself as a high-speed designer and I didn't want to let anyone down. I started using a high-speed design application and grew quite adept at it, but I still didn't consider myself a high-speed designer. I refined my existing high-speed skills, learned some new skills as well, and designed a great board. But I still didn't see myself as a high-speed designer.

Then, at the end of the design, I was congratulated on my high-speed design. Bing! The light went on and I realized that I was indeed a high-speed designer. Once again I had allowed the black spot of negative expectations to influence my thinking.

We obviously aren't going to do every little thing that we've ever dreamed of. I'm not going to be an astronaut or a Hollywood celebrity, and I'm pretty sure that I will never become Tony Stark's Iron Man. But there are many things out there that we can achieve professionally and personally that we don't try for because we have labeled ourselves with the black spot of negative expectations.

And in the same vein, the black spot of negative expectations can create great harm in our relationships and derail potential success, both professionally and personally. I believe that we would all benefit immensely by investing in a huge can of "black spot remover" and eliminating as many negative expectations as we can in our lives. Now, I think that I'll go and indulge myself in a big chunk of coffee cake. **PCBDESIGN**

Tim Haag is customer support and training manager for Intercept Technology.

Back to the Future: Science Fiction Turns Science Fact

Flying cars, hoverboards and video chat—a very futuristic vision for the year 2015 was presented in the movie "Back to the Future Part II", released in 1989. Now, shortly before "Back to the Future Day" on October 21, 2015, it is time to check whether reality has indeed kept up with the daring predictions of the '80s.

Marty McFly, the protagonist of the movie "Back to the Future Part II," uses a time machine to travel from the year 1985 to October 21, 2015. In the technological utopia of 2015 he is in for quite a few surprises. One of them is a colossal display on top of a cinema, from which a terrifying 3D shark seems to jump out to get him.

A first prototype has been developed by Tri-Lite Technologies and TU Wien a few months ago. Each 3D pixel (called "TrixelTM") consists of a laser and a moveable mirror. The mirror directs the laser beams across the field of vision, from left to right. With this basic idea, different pictures can be sent to the viewer´s left and right eye, so that a 3D effect is created without the need for 3D glasses.

"The software for controlling the modules and displaying movies has already been developed," says Jörg Reitterer (from Tri-Lite Technologies, and PhD student in Professor Ulrich Schmid's team at TU Wien). "We can use any off-the-shelf 3D movie and play it on our display."

Impact of Final Plated Finish on PCB Loss

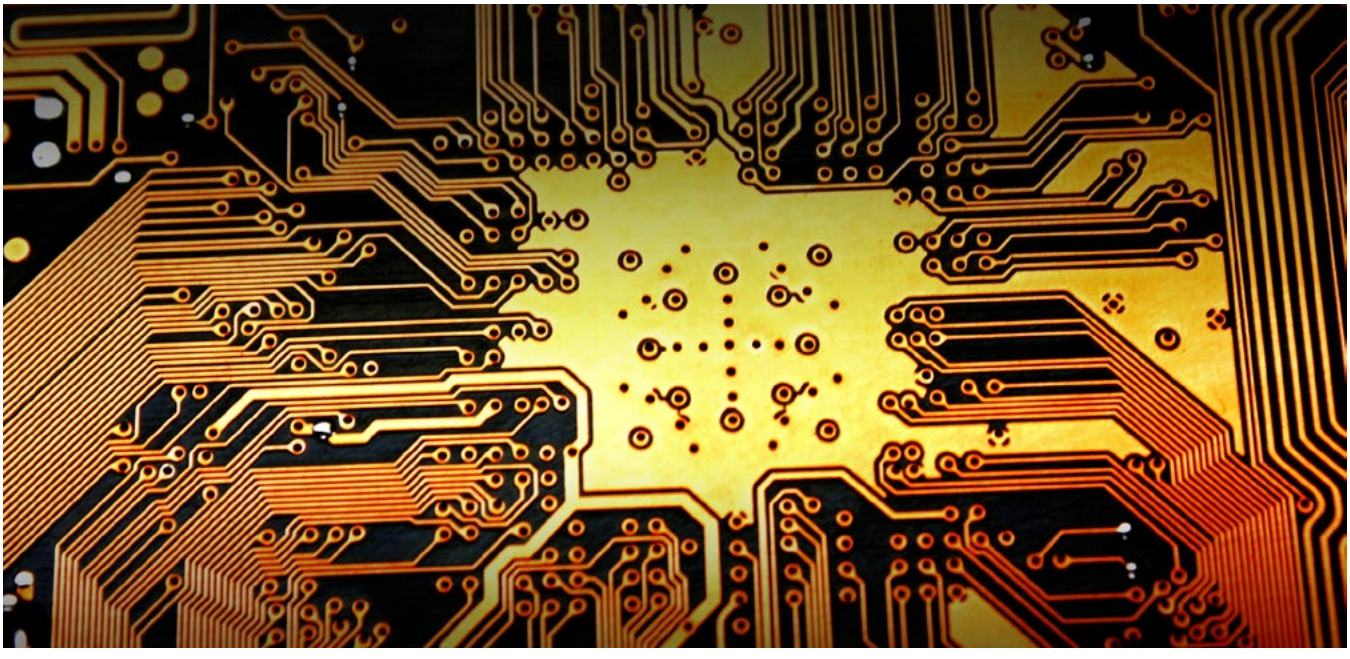
by John Coonrod
ROGERS CORPORATION

A variety of plated finishes are used in the PCB industry. Depending on the circuit construction and other variables, the plated finish can cause an increase in PCB insertion loss. The plated finish used on the outer ground planes of a stripline circuit have minimal or no impact on insertion loss. However, microstrip or grounded coplanar waveguide circuits, which are common on the outer layers of multilayer high-frequency PCBs, can be impacted by the plated finish for increasing the insertion loss.

In multiple experiments, comparisons were done between circuits with bare copper and circuits with different plated finishes. The bare copper circuits were used for reference only and the circuit structure was a microstrip transmission line circuit using substrates of different thickness.

The reason that most plated finishes cause increase insertion loss as compared to bare copper is that most plated finish are less conductive than copper. Electroless nickel/immersion gold (ENIG) is a very good finish. However, the simple fact is that nickel is about one-third the conductivity of copper, and a circuit with ENIG will have more insertion loss than the same circuit with bare copper. There are several variables concerning how much difference in insertion loss to expect and one of them is the substrate thickness. A substrate that is relatively thin will be more influenced by the conductor effects regarding insertion loss and the added plated finish will add to the conductor losses more for thin circuits than thick circuits. Conductor loss is one component of insertion loss.

A microstrip transmission line circuit is a simple structure with a signal conductor on the top layer and a ground plane beneath that layer. The microstrip transmission line circuit primarily has electric fields between the signal plane and ground plane, but there is a concentration of fields at the edges of the signal conductor. It



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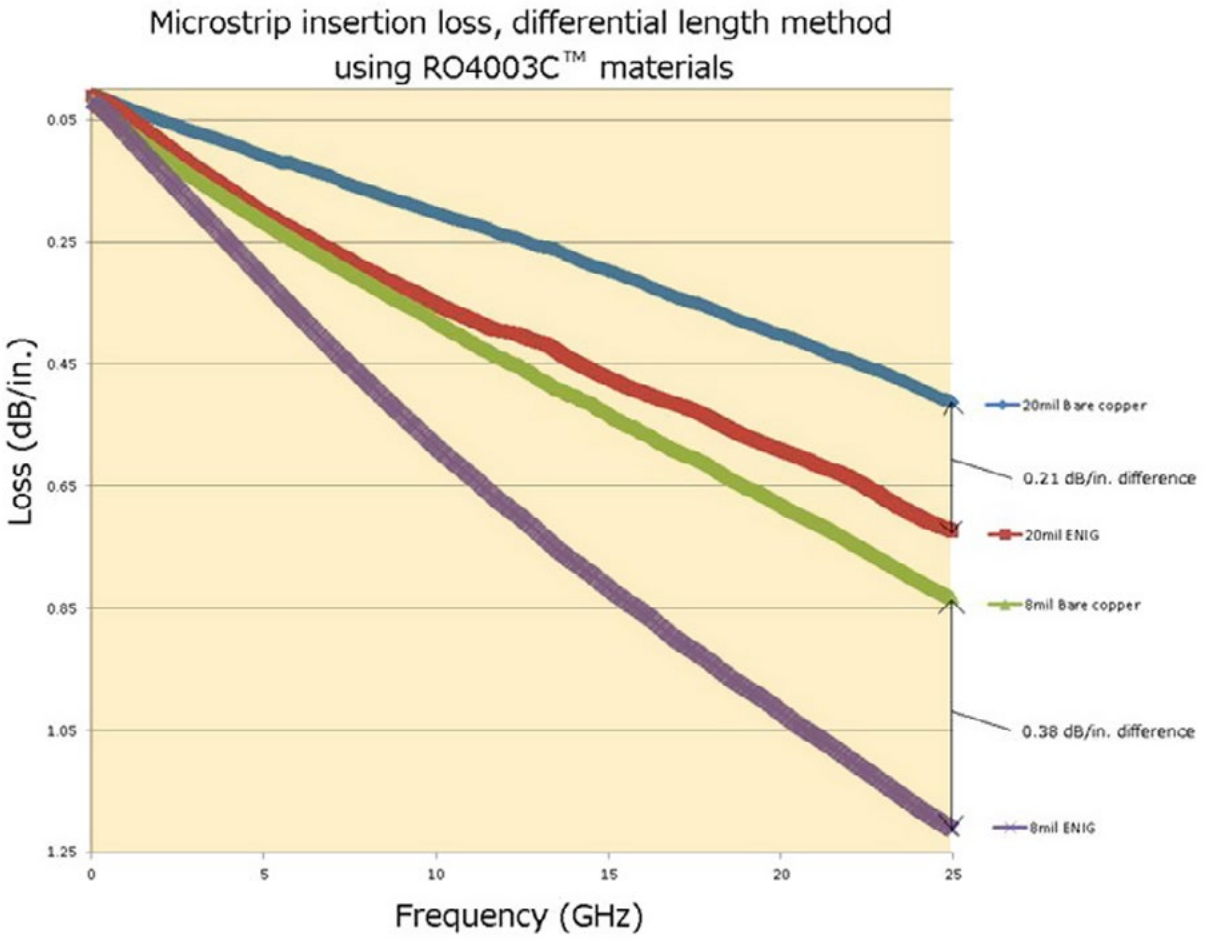


Figure 1: Results of experiment showing difference in insertion loss of microstrip transmission line circuit using bare copper and ENIG, with different substrate thickness.

is at the edges where the addition of the plated finish can increase the conductor loss, which will increase the insertion loss.

One experiment showed the difference in insertion loss of a microstrip transmission line circuit using bare copper and ENIG, but with different substrate thickness. It was found that the thinner circuits had a larger difference in insertion loss when comparing the circuits with bare copper to circuits with ENIG plated finish, as shown in Figure 1.

The material used in Figure 1 is RO4003C, a low-loss high-frequency circuit material. The dissipation factor for this material is 0.0027 when tested at 10 GHz in a clamped stripline test. If this same study used an FR-4 material (Df ≈ 0.020), the outcome would be very different, mainly due to the fact the FR-4 has about four times more insertion loss than RO4003C at 10 GHz and that additional loss is due to the dielectric loss. As an example, the same circuit using 20 mil FR-4 when tested at 10 GHz using bare copper has about 0.8 dB/inch insertion loss and Figure 1 shows the 20 mil RO4003C laminate with bare copper has an insertion loss of about 0.2 dB/inch at 10 GHz. The high dielectric loss of FR-4 makes the conductor loss much less significant, so the addition of a lossy plated finish will not be as obvious on FR-4 as it would on a low loss material.

As part of this plated finish study it was found that several finishes do not have much impact on insertion loss, when compared to a microstrip circuit using bare copper. Organic

solderability preservative (OSP) finish is typically thought of as a temporary finish and it does not have a significant impact on the insertion loss when compared to the same circuit using bare copper.

Another plated finish which showed no significant difference in insertion loss for this study was immersion silver. When considering the conductivity of raw silver it is actually one of the few plated finish metals which has higher conductivity than copper. However, the immersion silver process will deposit a very thin layer of silver on the copper conductor and due to skin depth the benefit of silver will not be realized except at higher frequencies. Still, it will not negatively impact insertion loss at the lower frequencies.

The other plated finishes considered were ENIG, ENIPIG and immersion tin. As stated before, these losses are dependent on the thickness of the circuit and the study evaluated microstrip transmission line circuits on a 5mil low-loss substrate to exaggerate the conductor effects of the added plated finish. In this study the circuits with the ENIG plated finish had the highest losses, then circuits using ENIPIG had less loss and the immersion tin circuits were lower.

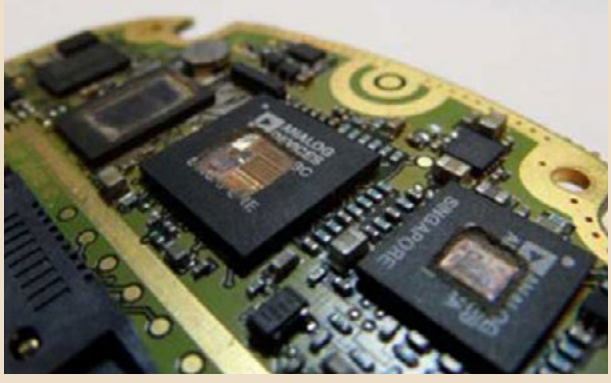
If more details from this study are desired, contact me and I'll be glad to provide an overview of the study. **PCBDESIGN**

John Coonrod is a senior market development engineer for Rogers Corporation. To read past columns, or to reach Coonrod, click here.

How Leaky is Your Device?

A new generation of digital devices that will protect consumers from cyber-attacks could be a step closer thanks to a grant of over £1 million from the Engineering and Physical Sciences Research Council (EPSRC) awarded to the University of Bristol for a research project to protect consumers' sensitive data.

Digital devices, such as smart banking cards or smart phones, are widely used to store private and sensitive data about peoples' digital lives. However, securing these devices is a major task for the computing industry. The research project by the University's Cryptography Research Group hopes to address the issue of leakage-related attacks.



Information leakage via side channels is a widely recognised threat to cyber security. In particular small devices are known to leak information through physical channels, i.e., power consumption, electromagnetic radiation, and timing behaviour. In other words, the power consumed by mobile phones can reveal information about the data stored on the phone and attackers can steal this data by managing to capture the leakage.

Dr. Elisabeth Oswald, Reader in Applied Cryptography in the Cryptography Research Group and who is leading the project, said: "Our previous research has shown that in the case of small embedded devices, the nature of the leakages can be appropriately modelled using statistical tools.

"This project's research hypothesis is that one can make meaningful statements about the leakage behaviour of new implementations on such small devices by utilising a priori derived models."

As the world gets even more digital, and attackers become more sophisticated, this is another important step on the arms race between the good guys and the bad guys.

MilAero007 Highlights

ELCOSINT—The Future of High-Temperature Interconnect

The increasing need for electronic assemblies to endure high-temperature operating conditions in aerospace, automotive, oil and gas drilling, power management and renewable energy applications, whether those conditions involve high ambient temperatures, high cycle temperatures or high junction temperatures, is driving the development of high-temperature interconnection technologies.

Fortifying Computer Chips for Space Travel

Space is cold, dark, and lonely. Deadly, too, if any one of a million things goes wrong on your spaceship. It's certainly no place for a computer chip to fail, which can happen due to the abundance of radiation bombarding a craft. Worse, ever-shrinking components on microprocessors make computers more prone to damage from high-energy radiation like protons from the sun or cosmic rays from beyond our galaxy.

Sensor Data Fusion Offers Countermeasures Against Small Drones

Airbus Defence and Space has developed a counter-UAV system which detects illicit intrusions of Unmanned Aerial Vehicles (UAVs) over critical areas at long ranges and offers electronic countermeasures, minimizing the risk of collateral damage.

NASA is Laser-focused on Deep Space Communication

Today's technology has all but eliminated time delays in telecommunication on Earth, but when they do occur they can be frustrating, especially when trying to communicate complex or time-sensitive information. The same type of delay could happen when communicating with spacecraft and crew members in deep space on the journey to Mars.

China Now Third Largest Importer of Defence Equipment

China's defence budget is expected to almost double by the close of this decade, according to a new analysis released today by IHS Inc., the leading global source of critical information and insight.

Self-healing Material Could Plug Life-Threatening Holes in Spacecraft

For astronauts living in space with objects zooming around them at 22,000 miles per hour like rogue super-bullets, it's good to have a backup plan. Although shields and fancy maneuvers could help protect space structures, scientists have to prepare for the possibility that debris could pierce a vessel.

The Drones Report 2015

The fast-growing global drone industry has not sat back waiting for government policy to be hammered out before pouring investment and effort into opening up this all-new hardware and computing market.

Advancing Bio-inspired Micro-robotics Technology

BAE Systems will have a significant role working with the MAST Alliance's team of scientists from the U.S. Army, academia, and industry as it advances bio-inspired micro-robotics technology to extend the remote sensing capability of U.S. ground forces. "The technologies being developed under MAST will support products that extend soldiers' capabilities while keeping them out of harm's way," said Bill Devine, MAST's strategic development manager for BAE Systems.

Construction to Begin on World's Largest Camera

The Department of Energy has approved the start of construction for a 3.2-gigapixel digital camera—the world's largest—for the Large Synoptic Survey Telescope.

Teeny Tiny Guardians of Our Chips

Counterfeit, cloned, and otherwise doctored electronic chips already are circulating in markets and the problem is only likely to grow in the coming years. Shown here are dummy "dielets" that DARPA-supported researchers have produced to help them learn how to dice, sort, pick, place and otherwise handle such teensy components, which would affix to individual chips with a footprint the size of a dust speck.

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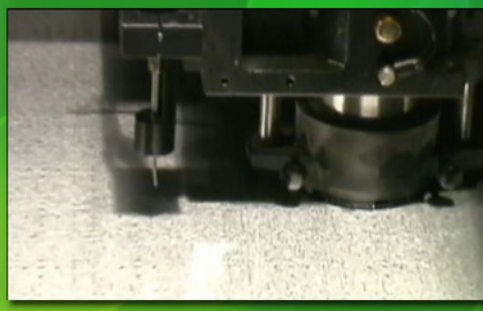

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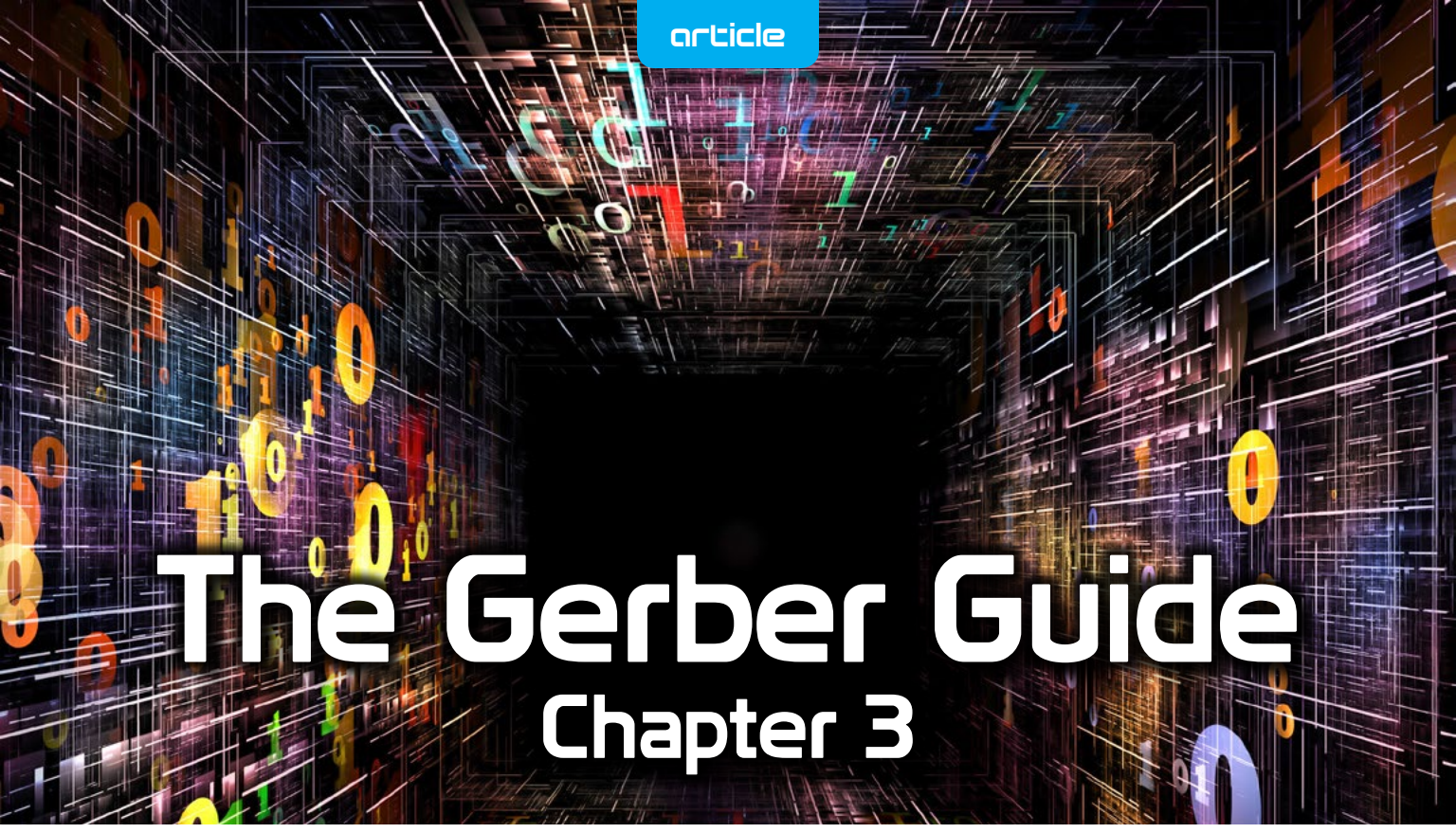

The Gerber Guide
Chapter 3

by Karel Tavernier
UCAMCO

It is possible to fabricate PCBs from the fabrication data sets currently being used; it's being done innumerable times every day all over the globe. But is it being done in an efficient, reliable, automated and standardized manner? At this moment in time, the honest answer is no, because there is plenty of room for improvement in the way in which PCB fabrication data is currently transferred from design to fabrication.

This is not about the Gerber format, which is used for more than 90% of the world's PCB production. There are very rarely problems with Gerber files themselves; they allow images to be transferred without a hitch. In fact, the Gerber format is part of the solution, given that it is the most reliable option in this field. The problems actually lie in which images are transferred, how the format is used and, more often, in how it is not used.

In this monthly series, I will explain in detail how to use the newly revised Gerber data format to communicate with your fabrication partners clearly and simply, using an unequivocal yet versatile language that enables you and them to get the very best out of your design data. Each month we'll look at a different aspect of the design to fabrication data transfer process. This month we'll look at the PCB profile, or outline.

Chapter 3: The PCB Profile (or Outline)

The profile defines the extent of the PCB. It separates the PCB from what is not the PCB and is an essential part of PCB fabrication data. Without the profile, the PCB simply cannot be fabricated. The profile must be properly and precisely defined.

The profile defines a simple region in the 2D plane. The proper way to do this is to specify a closed contour: The inside of the contour is the PCB, and the outside is not. It is that simple.

Note that such a simple region is solid, without holes. By definition then, a profile cannot have holes intentionally placed within it. These are superfluous and represent an unnecessary and complicated duplication given that drill holes are well defined in the drill/rout file. One can view cut-outs in a PCB as still part of the PCB, just as much as the drill holes are.

A contour is defined by the Gerber spec as follows:

"A contour is a sequence of connected draw or arc segments. A pair of segments is said to connect only if they are defined consecutively, with the second segment starting where the first

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October 13–15
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- Best Practices in Assembly
- Advanced PCB Troubleshooting
- SMT Problem Solving

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IPC Flexible Circuits-HDI Conference
Minneapolis, MN, USA
Presentations will address Flex and HDI challenges in methodology, materials, and technology.

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Figure 1: Profile defined by G35/G37 region.

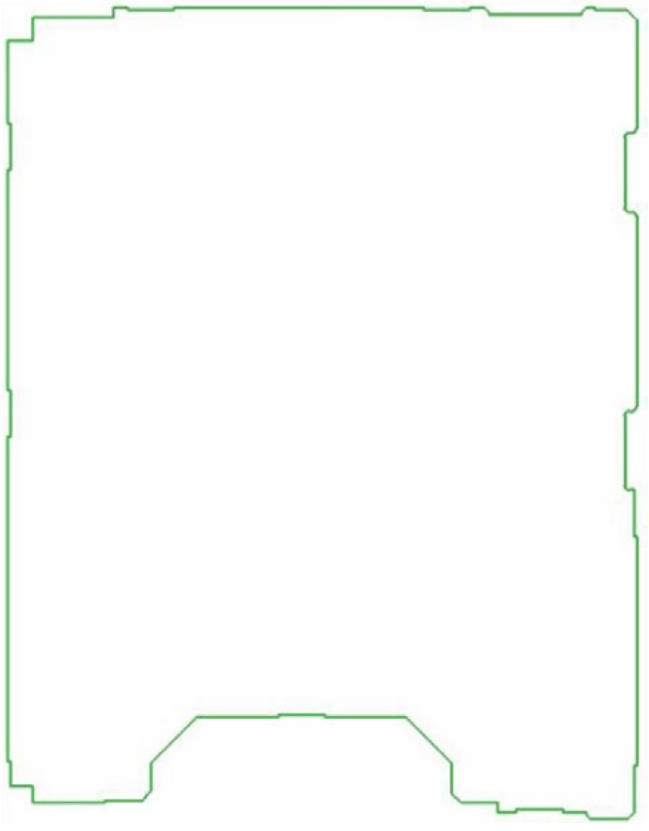


Figure 2: Profile stroked with a thin aperture.

one ends. Thus the order in which the segments of a contour are defined is significant. Non-consecutive segments that meet or intersect fortuitously are not considered to connect. A contour is closed: The end point of the last segment must connect to the start point of the first segment."

The Gerber format regions are defined by contours using the G36/G37 commands. This is precise and unequivocal, and is the recommended way to specify the profile. The filled contour covers the PCB exactly.

If this is not possible, the profile can be specified by drawing the contour with a zero size or very small size aperture. If the aperture is not zero size, the profile is the center line of the stroked line; in other words, do not compensate for aperture size. You are transferring an image, not a production tool for a drill machine. The profile layer is not copper. It is more akin to a drill or rout file as it affects all layers. The outline should therefore be put into a separate file, and not shoved into a copper layer.

It is helpful to provide a mechanical drawing with the profile. However, this is not a substitute for digital data.

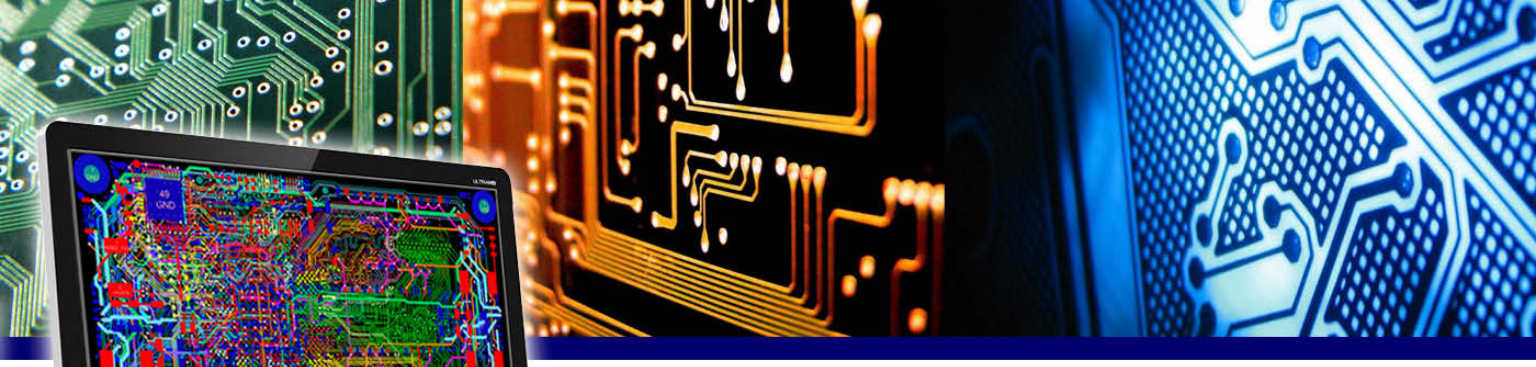
Corner marks are sometimes used to indicate the profile. Again, corner marks are meant for visual interpretation and do not constitute digital data. Therefore, they are not a valid specification of the profile.

What is definitely unacceptable is to take a copper layer and add a crude manually-drawn line that, to make matters worse, is drawn with the same aperture as the copper tracks.

Next month we'll move on to Chapter 4. See you then. **PCBDESIGN**

This column has been excerpted from the Guide to PCB Fabrication Data: Design to Fabrication Data Transfer.

Karel Tavernier is managing director of Ucamco.



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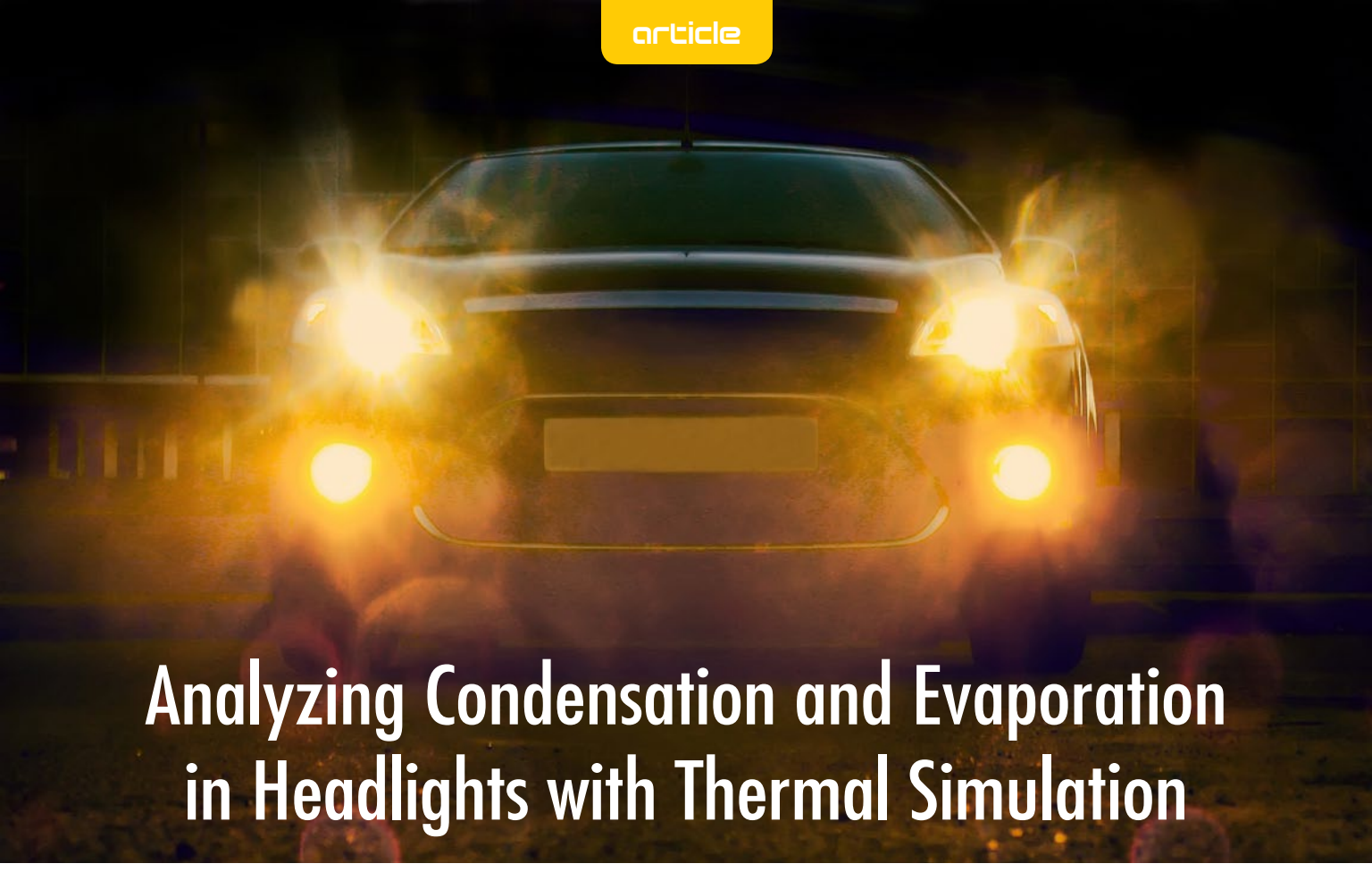

Analyzing Condensation and Evaporation in Headlights with Thermal Simulation

by Boris Marovic and John Wilson
MENTOR GRAPHICS CORPORATION

The only constant in automotive lighting design seems to be the need for thermal management. This task is often done with computational fluid dynamics (CFD) simulation software because creating prototypes for each design iteration is slow and costly. Traditional CFD simulations are done by analysts who have specialized skills in advanced mathematics and fluid dynamics, plus a command of the complex modeling tools required for CFD work. The analyst has to assign grids to the solids and flow spaces, creating an optimized computing mesh. This mesh aids in setting boundary conditions and influences the solution convergence as well as accuracy of the result.

CFD mesh generation for creating an accurate thermal model of a new lighting system is time-consuming. Even before the mesh is generated, the geometry from the CAD model has to be simplified to be able to run CFD analysis. The actual geometry of a headlight includes many fine details, such as the saw-tooth structure of the light guides, small ribs on the reflector, bezels for the stray light creation onto the road signs above the road, or the small facetted surfaces of the orange plastic on the turning signal light. These structures are a challenge to tackle in the meshing process. And typically, when the CFD mesh is finally completed after several days of manual work, the design is

Figure 1: Automotive headlights have to function in harsh and variable conditions.

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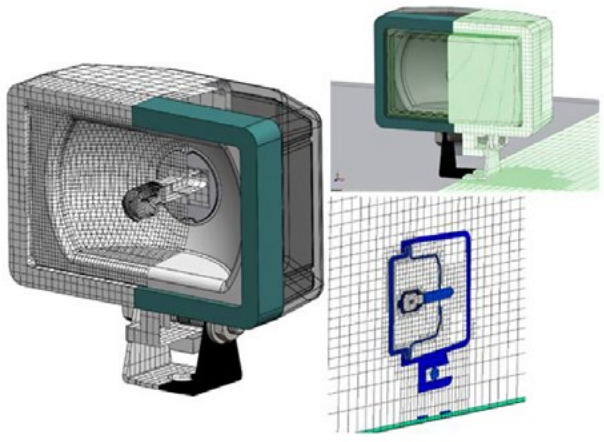

Figure 2: CFD Mesh needed to model the headlight in thermal simulations.

changed slightly before the first thermal simulation gets to run.

Thermal simulation is critical to avoid any damage to the lighting system caused by either environmental impacts, such as solar radiation, or a poorly designed system. A fan that is used for cooling high-bright LEDs could create a thermal short-circuit—when the hotter air that comes out of the heatsink from the LEDs is sucked back into the fan and reused, drastically reducing the cooling efficiency. The result is an even hotter LED junction temperature and a damaged system. In the physical assembly, fixing this flaw is costly and time-consuming, and it's unnecessary when the error can be easily caught within the simulation before the physical model is created.

New CFD technologies are available that can move thermal simulation further up in the design process, automate laborious analytical tasks, and eliminate the need for geometry simplification. This type of CFD software, such as FloEFD®, integrates directly with MCAD tools, which enables design engineers to match the thermal simulation with the latest design iteration. It also provides automatic meshing, which speeds up the entire thermal simulation process. However, accuracy should not be sacrificed in the name of faster simulations. The corresponding physics must be represented in the simulation with a highly accurate result compared to physical prototype experiments.

Thermal simulation for automotive lighting designs needs to address extreme and critical operating issues; for example, a car leaves a relatively humid warm garage after a rainy day and goes into the cold outside the following day and an undesirable condensation film starts to build up on the front lens of the lighting system. Simulation of this situation requires certain capabilities in the software such as a Monte Carlo radiation model and condensation calcu-

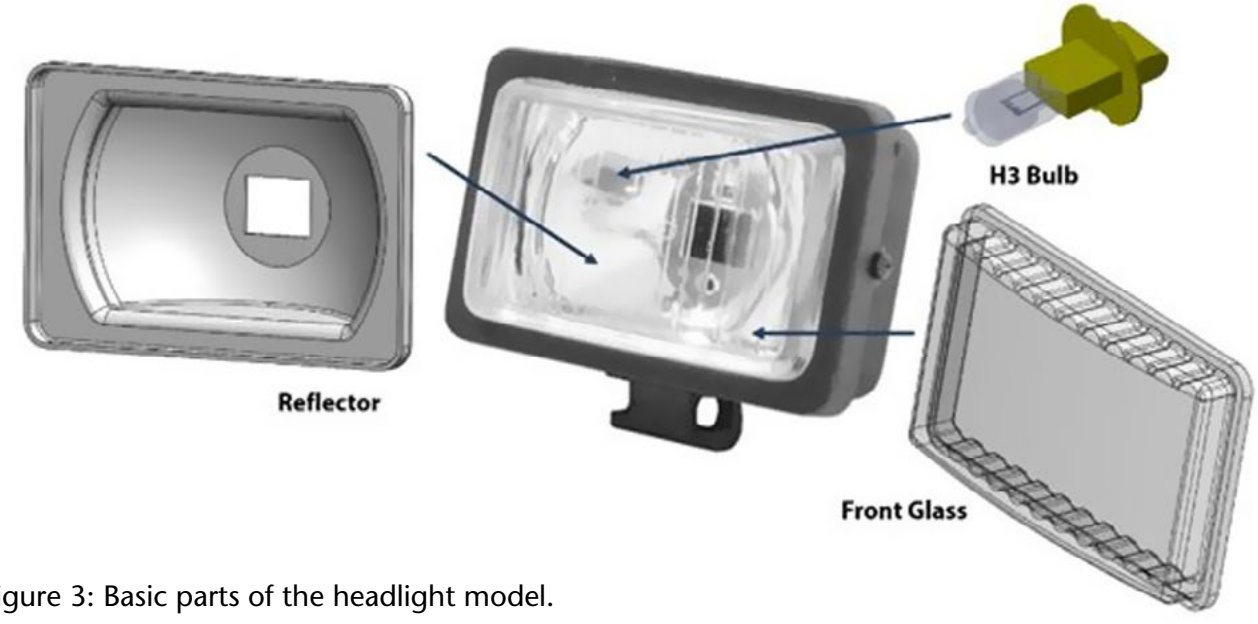

Figure 3: Basic parts of the headlight model.

lation in which a transient simulation can provide information on how fast and where the condensation will disappear. It should also be able to show how evaporation could be improved with specific design changes.

Case Study

The following is a real-world CFD analysis on an LED-based headlight (Figure 1) using the condensation and radiation models in FloEFD. In this experiment, the initial conditions for the model of the inside of the headlight were a temperature of 50°C, pressure at 1 atm, and relative humidiy of 95%. The external conditions were set at -10°C and 50% relative humidity. The inner and outer surfaces of glass were assigned to be "wettable." The CFD software was used to simulate a warm headlight initially placed into a cold environment, with the headlight off for 30 minutes and then turned on. Figures 3-5 show the product specifications used for this simulation.

During the cooling phase, starting at about 1,000 seconds from the beginning of the 30 minutes, the temperature in various regions dropped below 0°C, and freezing (crystallization) of the film occurred. Between the start of the crystallization and the switching on of the bulb (1,800 seconds from the start) a minor decrease in the film mass caused by evaporation and sublimation was observed. Once the bulb was switched on, removal of the condensation film occurred. The processes of melting and subsequent evaporation lasted no more than 300 seconds. An additional 1,800 seconds were needed to obtain a steady thermal state of the headlight. Figure 6 shows the change in the film's thickness and contours over time.

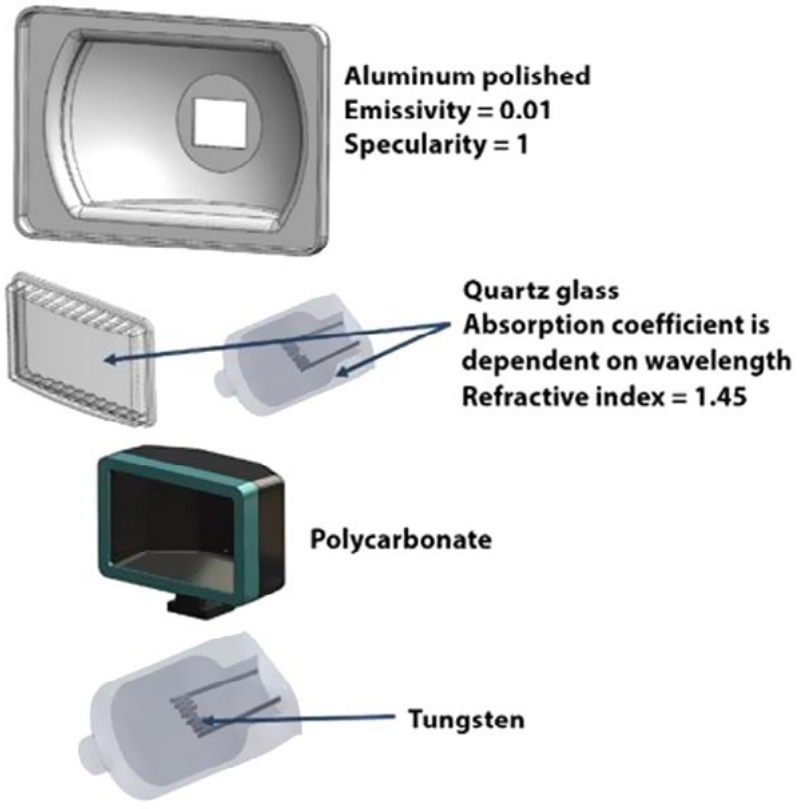

Figure 4: Materials that need to be considered when creating the model.

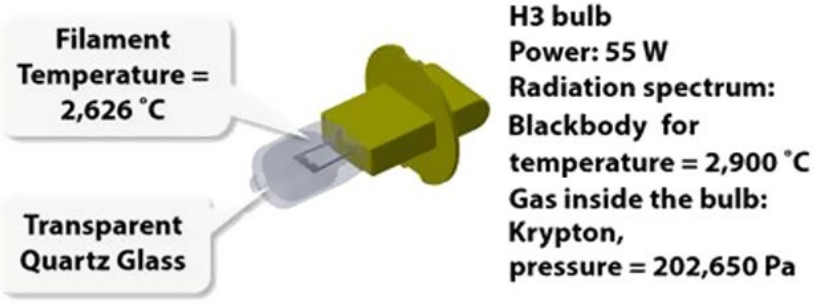

Figure 5: The LED specifications used in this model.

Although the condensation film mass and its average thickness decreased after switching on the bulb, the film thickness still increased on local regions on the glass. This was evidence of the vapor transport within the headlight's internal space; that is, the evaporated mass from the hotter regions of the surface is condensed on the relatively colder ones. Condensation film motion was observed as a

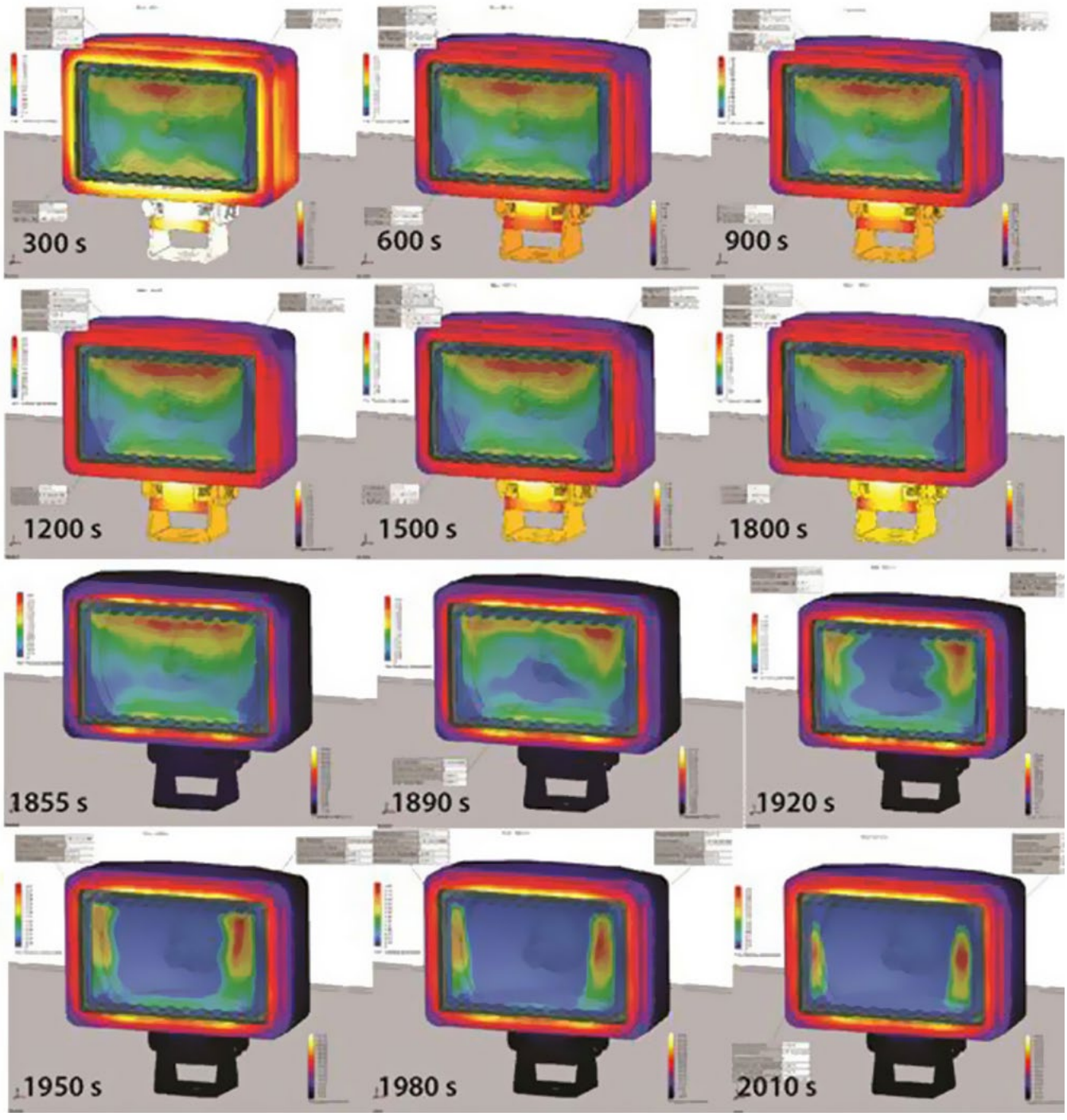

Figure 6: Simulation results of the changes in the condensation film thickness and contours that occurred over 30 minutes.

result of gravitational forces (Figure 7). At 900 seconds, just before crystallization began, the maximum value of the film velocity was about 1.1 mm/min.

The mathematical model of surface condensation and evaporation was useful in performing transient simulations of film formation and removal. Several problems were considered to validate the model, and there was good agreement with the experimental data [1].

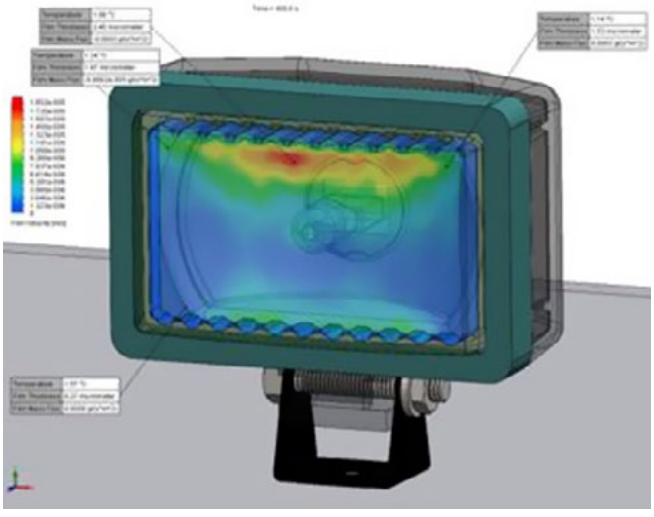

Figure 7: The thermal simulation also shows the movement of the condensation film caused by gravity.

Vapor condensation and evaporation on a headlight's surface is crucial to its operation, and today's CFD tools allow thermal analysis of the headlight's design to be done in days, rather than weeks, helping to shorten the time from concept to production. The ability to account for the change of a film's thermal state and thickness caused by the heat exchange with the external fluid flow and the solid body, surface evaporation/condensation, melting/crystallization within the film volume, and motion caused by gravitation and friction forces from outer flow is particularly useful. **PCBDESIGN**

References

1. G. Dumnov, A. Ivanov, A. Muslaev, M. Popov, and J. Christopher Watson, "Evaluating Water Film and Radiation Modeling Technologies in CFD for Automotive Lighting," NAFEMS NWS World Congress 2015, 21–24 June, San Diego, California.

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John Wilson is a technical marketing engineer at Mentor Graphics Corporation. He received his BS and MS in Mechanical Engineering from the University of Colorado at Denver. Since joining the company in 1999, he has worked on or managed more than 100 thermal and airflow design projects.

Energy Out of Thin Air

Lithium-air batteries could be the next big thing, if it wasn't for their very short lifetime. But an EU-funded project has doubled it.

Since they were first commercialised in 1991, lithium-ion batteries have come a long way. But as the machines they power become greedier, engineers have had to start looking into alternatives with a higher storage capacity. One of these alternatives resides in lithium-air (Li-air) technology—batteries consisting of metal-based anode and air-cathode which constantly extract oxygen from the ambient air.

"The main advantage of a lithium-air battery is its high energy density, which is theoretically 10 times higher than that of lithium-ion batteries," explains Professor Qiuping Chen, associate Professor at the Polytechnic University of Turin and coordinator of the STABLE project.

STABLE's objective: increasing this capacity from 50 to 100-150 cycles and demonstrating this breakthrough in functional cells within three years. "The project is a complete success in this regard, with a life that has reached 151 cycles," enthuses Chen.

TOP TEN

Recent Highlights from PCBDesign007

1 Mentor Graphics' Wally Rhines Recognized with 2015 Phil Kaufman Award

A member of the EDAC Board of Directors since 1994, Dr. Rhines served an unprecedented five two-year terms as EDAC's chairman over a 16-year period from 1996 to 2012. "Dr. Rhines has helped drive EDAC to a position of leadership, creating a mechanism for the EDA industry to grow and address common issues," remarks Robert P. Smith, executive director of EDAC.

2 Failure Mode: Hole Wall Pullaway

This column is based on my experience in test reliability of interconnect stress test (IST) coupons. I am addressing HWPA that features moderate to severe outgassing. There may be HWPA due to thermal stressing of the board without any significant outgassing, but this type of HWPA is subtle, and it presents as a dark line between the plating and the dielectric of the hole wall. This type of HWPA is rarely detected.

3 Intercept Unveils Enhancements to Pantheon Ink Resistor Technology

"Enhancements to Pantheon's ink resistor functionality combine the power of Pantheon's PCB/Hybrid/RF design flow with the intuitive setup and modification of complex ink resistor shapes for the highest advancements in design layout and geometry creation," said Dale Hanzelka, director of sales and marketing at Intercept.

4 The Reindustrialization of Europe

With an inquisitive mind and a head for challenges, besides the ability to think outside the box and the courage to dare to be different and strive to be first, Spirit Circuits MD Steve Driver can be relied upon to grab the attention of an audience of PCB professionals. As keynote speaker at the Institute of Circuit Technology Hayling Island Seminar, he lived up to his reputation with a motivational presentation, the two themes of which exemplified his latest entrepreneurial venture.

5 Material Witness: Using Scaled Flow Data

The IPC TM-650 Scaled Flow Test (2.4.38) uses three values to determine pressed thickness and flow of a given resin system: Ho (the theoretical value of a pressed sample assuming no air entrainment and no flow calculated from the weight of the test stackup), Hf (the actual final thickness per ply measured by micrometer after the flow test) and ΔH (the difference between Ho and Hf expressed in mils of thickness change).

6 Automotive Systems Design: a Support Engineer's Perspective

Assume you need to design a multipart complex product requiring several PCBs to be fitted into a tight housing. Assume also that you have to bring product iterations to market as fast as possible, be it at regular intervals or on demand. Finally, assume that you will have to do this not only faster, but also at an increasingly lower cost. This is a trend that becomes the norm for products in many industries, not least in automotive electronics.

7 EDA Industry Revenue Up 8.5% in Q2, But PCB Drops

The EDA Consortium (EDAC) Market Statistics Service (MSS) has announced that the EDA industry revenue increased 8.5 percent for Q2 2015 to $1.9 billion, compared to $1.75 billion in Q2 2014. But PCB and MCM revenue dropped 13 percent compared to Q2 2014. The four-quarters moving average, which compares the most recent four quarters to the prior four quarters, also increased by 8.5 percent.

8 Herbstman, Holden and Kowalewski to Lead Denmark HDI Workshop

This workshop is for all PCB layout designers who see the need to achieve 2X to 4X higher board density, better electrical performance, or even those who just need to reduce the size or thickness of a finished board. This class is essential for those who use HDI, but it is not limited to HDI designers. So, if you want to learn how to use HDI or just be better at it, come learn from the best.

9 Kelly Dack and Mark Thompson Unite in War on Failure

There's been a lot of talk about fighting the war on failure in the PCB industry. But what strategies should our generals follow to prosecute this war? What exactly constitutes a failure in the first place? Is this war even winnable? I recently spoke with longtime designer Kelly Dack and CAM support veteran Mark Thompson of Prototron Circuits about the best battle plans for beating failure.

10 The Gerber Guide, Chapter 22

Never mirror or flip layers! All layers must be viewed from the top of the PCB, which means that the text must be readable on the top layer and mirrored on the bottom layer. Alas, sometimes, in a mistaken attempt to be helpful, designers flip layers because they must anyway be mirrored on the photoplotter. This could be helpful in a world where the designer's files are used directly in fabrication, but these data layers are actually input for the CAM system.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out ***The PCB Design Magazine's*** event calendar.

IPC Europe Forum: Innovation for Reliability
October 13–15, 2015
Essen, Germany

14th International Symposium on Microelectronics Packaging (ISMP 2015)
October 13–15, 2015
Seoul, South Korea

International Wafer-Level Packaging Conference
October 13–15, 2015
San Jose, California, USA

Long Island SMTA Expo and Technical Forum
October 14, 2015
Islandia, New York, USA

TPCA Show 2015
October 21–23, 2015
Taipei, Taiwan

LED Assembly, Reliability & Testing Symposium
November 17–19, 2015
Atlanta, Georgia, USA

Rapid Oven Setup & PCB Profiling – Seminar
November 24, 2015
Warwickshire, UK

2015 International Printed Circuit & APEX South China Fair
December 2–4, 2015
Shenzhen, China

DesignCon 2016
January 19–21, 2016
Santa Clara, California, USA

IPC APEX EXPO Conference & Exhibition 2016
March 15–17, 2016
Las Vegas, Nevada, USA

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